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transforming specialty electronics

MYXPM6021*

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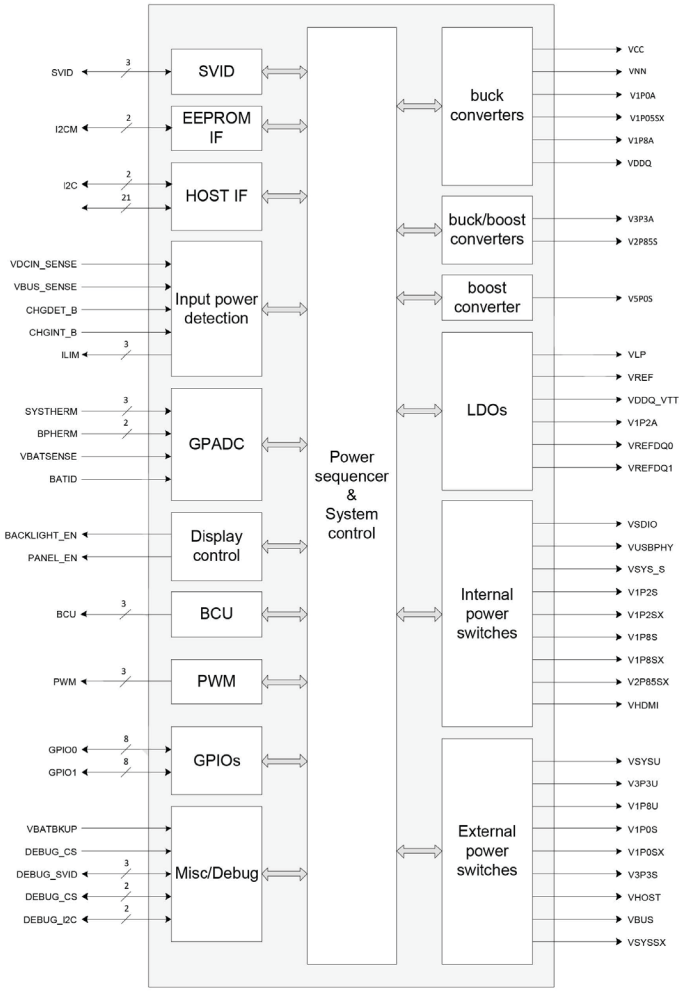
Power Management IC (PMIC)

Features

- Intel® Atom Bay Trail PMIC
- Tin-lead ball metallurgy
- Part number MYXPM6021
- Two high efficiency buck converters with integrated SVID interface running IMVP-7 protocol. These two quad phase DC/DC regulators generate the voltages for CPU and graphic cores
- One dual phase buck regulator for memory supply supporting DDR3-L and -LP memory types
- 3 single phase buck regulators supplying 1.0V, 1.05V and 1.8V towards the platform
- 2 buck-boost converters generating 2.85V and 3.3V for the platform even if the input supply is down to 2.7V
- Boost converter providing 5V for the USB components
- 3 LDOs with fixed output voltage
- 2 LDOs with programmable output voltage
- 1 push-pull LDO used for DDR3 address line termination
- 11 integrated power rail switching devices
- 9 external power rail switching devices
- Ultra flexible power sequencer programmable via OTP/ EEPROM and register
- I2C communication interface for SoC access
- EEPROM interface for optional OTP over-writing
- 16 general purpose I/Os with alternate functions
- 16 channel 10-bit ADC including conditioning circuits and programmable flexible sequencing for automatic and manual measurements
- System voltage and temperature monitoring, supervising
- Programmable IRQ controller
- 1-wire digital battery interface including 2-wire conversion
- 3 channel PWM signal generation, flexible frequency and duty cycle programmable
- Input power source detection, included with charger control
- 325 ball FCBGA 11mm x 6mm, 0.4mm pitch package
- Operating Temp Range: -30C - +85C



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1 General Description

The MYXPM6021 PMIC is a monolithic single chip power management IC for the next generation Intel® Atom™ processor. It provides all power supplies for tablet PC's and can also be used in multiple embedded applications as well as Netbooks and Nettops. It is designed to support platforms based on Intel's new Atom processor series, including DDR3 memory and various peripherals.

Integrated Power Management

Micross' new MYXPM6021 uses a single supply voltage at a wide range of input voltage and provides low noise supplies to all SoC voltage domains, DDR3 memory and many peripherals. The MYXPM6021 integrates 6 high performance low dropout (LDO) voltage regulators using Micross' patented Smart Mirror™ technology for very low quiescent current. It includes 11 internal power switches and the control logic for 9 external switching devices. These include in-rush current control for platform power distribution simplification. Six fully integrated high efficiency DC-DC buck converters provide current to Intel Atom platform's various low voltage domains as well as to the memory and the peripherals. Two buck-boost and one boost converter also supply energy for the platform. All nine regulators are designed to support external component height of 1mm.

Ultra Flexible Power Sequencer

The ultra-flexible power sequencer takes care of the complete platform start-up, state-transitioning and power down procedure. The MYXPM6021 operates autonomously and reduces the power consumption when entering stand-by or power down mode. The MYXPM6021 is fully programmable and allows adaption to all Intel Atom processor and platform sequences. The OTP programmed power sequence is copied into operational registers during power-up. Those registers can be overwritten by EEPROM after initial OTP copy routine or via operational processor.

Auxiliary Function

An analogue to digital converter (ADC) with 10-bit resolution combined with a multi-channel input multiplexer allows measurement of the input supply voltage, battery ID, PMIC die temperature, as well as 5 battery pack and system temperatures. The number of external components is significantly reduced due to the integration of 16 GPIO's, 3 channel PWM output signal generators, a multi-input detector with a charger control, as well as a programmable IRQ controller.

2 Key Features

- Two high efficiency buck converters with integrated SVID interface running IMVP-7 protocol. These two quad phase DC/DC regulators generate the voltages for CPU and graphic cores.
- One dual phase buck regulator for memory supply supporting DDR3-L and -LP memory types
- 3 single phase buck regulators supplying 1.0V, 1.05V and 1.8V towards the platform
- 2 buck-boost converters generating 2.85V and 3.3V for the platform even if the input supply is down to 2.7V
- Boost converter providing 5V for the USB components
- 3 LDOs with fixed output voltage
- 2 LDO with programmable output voltage
- 1 push-pull LDO used for DDR3 address line termination
- 11 integrated power rail switching devices
- 9 external power rail switching devices
- Ultra flexible power sequencer programmable via OTP/ EEPROM and register
- I2C communication interface for SoC access
- EEPROM interface for optional OTP over-writing
- 16 general purpose I/Os with alternate functions
- 16 channel 10-bit ADC including conditioning circuits and programmable flexible sequencing for automatic and manual measurements
- System voltage and temperature monitoring, supervising
- Programmable IRQ controller
- 1-wire digital battery interface including 2-wire conversion
- 3 channel PWM signal generation, flexible frequency and duty cycle programmable
- Input power source detection, included with charger control

3 Overview

MYXPM6021 features:

- Power Sequencer & System Control: MYXPM6021 includes an ultra-flexible power sequencer programmable via OTP during manufacturing process and modifiable via external EEPROM data. It controls the MYXPM6021 blocks, the power sequences, the programmed ADC sequence, interacts with the SoC and the peripherals
- Supply Sources
  - 6 Buck Regulators
  - 2 Buck-Boost Regulators
  - 1 Boost Regulator
  - 6 LDO Regulators
  - 11 internal power rail switches
  - 9 external power rail switches
  - 2 Power mux switches where the supply source can be selected
- Communication Interfaces
  - I2C (slave device) mastered from the SoC
  - Handshake/control signals from/towards the SoC and peripherals
  - SVID (slave device) mastered from the SoC, but capable of interrupt from the PMIC
  - I2C (master device) or EEPROM Interface, used to read EEPROM during first power up.
- Input Source Power Detection: MYXPM6021 will detect connected power sources and provide such information towards the SoC and/or charger. VBAT, VBUS_SENSE, VDCIN_SENSE and VSYS nodes will be permanently monitored via comparators for insertion, removal events. Furthermore they will be measured via the GPADC in order to take decision on the boot process.
- System Voltage and Temperature Measurement: The sytem voltage and temperature measurement monitors the MYXPM6021 input voltage at VSYS, the on-die temperature as well as the battery and platform sensor temperatures. In addition, it detects over- and under-voltage conditions. If activated, it can issue critical events.
- GPADC: The GPADC is primarily for temperature and voltage measurements, and can run predefined sequences or a single programmable one. It also supports automatic and manual measurement methods and can also run also in a standby mode at programmable long intervals.
- Digital Battery Interface: 1-wire protocol agnostic digital communication between battery and SoC. It introduces a level shifting between the SoC and the main battery.
- OTP & EEPROM Interface: MYXPM6021 will read its parameters from integrated OTP during power on reset. Optionally those OTP parameter settings can be overwritten by an external EEPROM for back-up solution, debugging or development. Note, The OTP can’t be overwritten and the EEPROM can’t be programmed via the MYXPM6021.
- Platform Back-up Battery Charger: MYXPM6021 includes an autonomous charger for platform backup batteries such as coin cells or “supercaps”.

- Display Control:
  - BCU: Battery controller unit, supervising peripherals based on system voltage.
  - PWM: The MYXPM6021 can generate up to 3 PWM signals with programmable duty-cycle and frequency to accommodate some external functionality.
  - GPIOs: 16 general purpose I/O with alternate functions.

4 Block Diagram

Figure 1: Overview Diagram

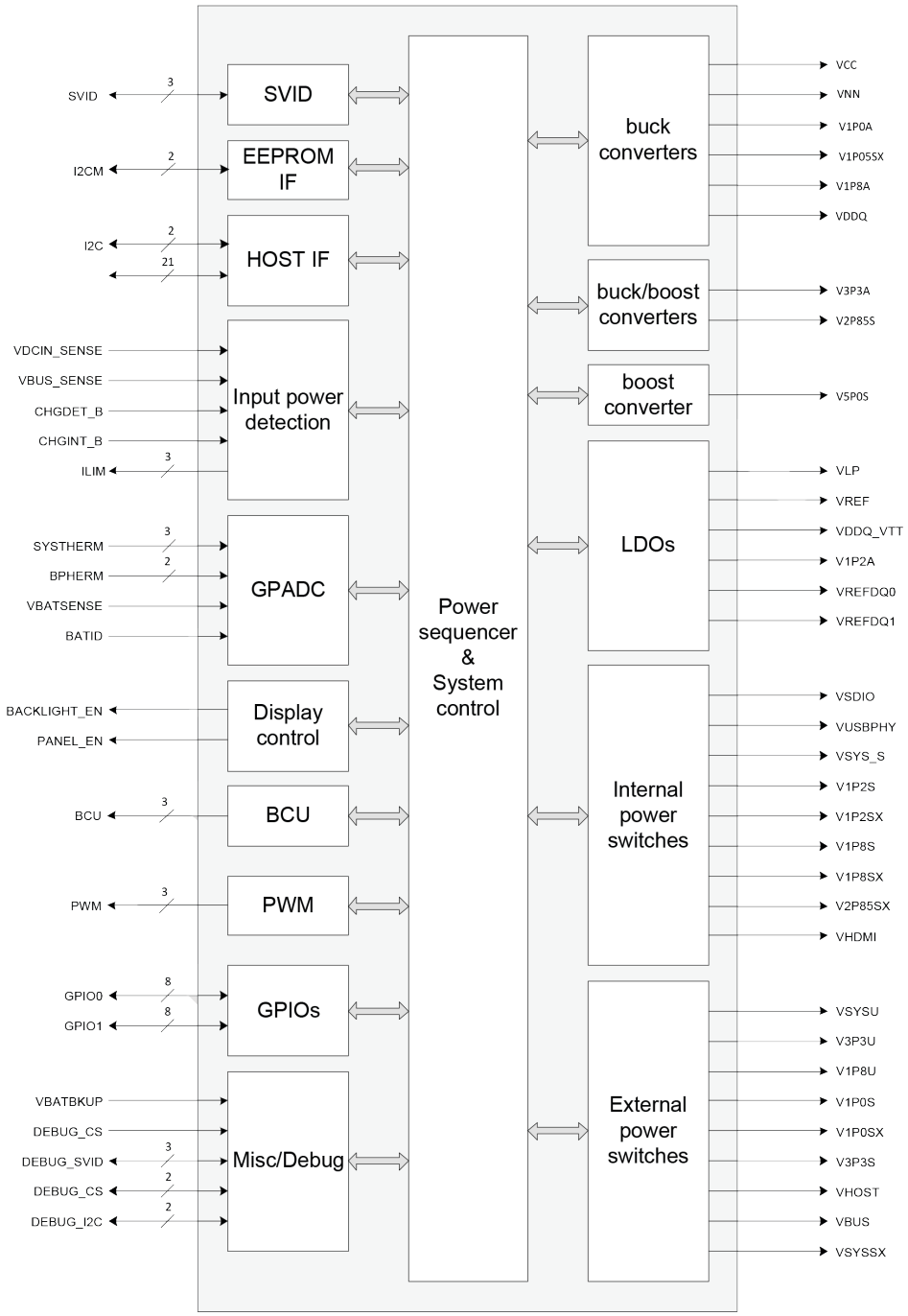

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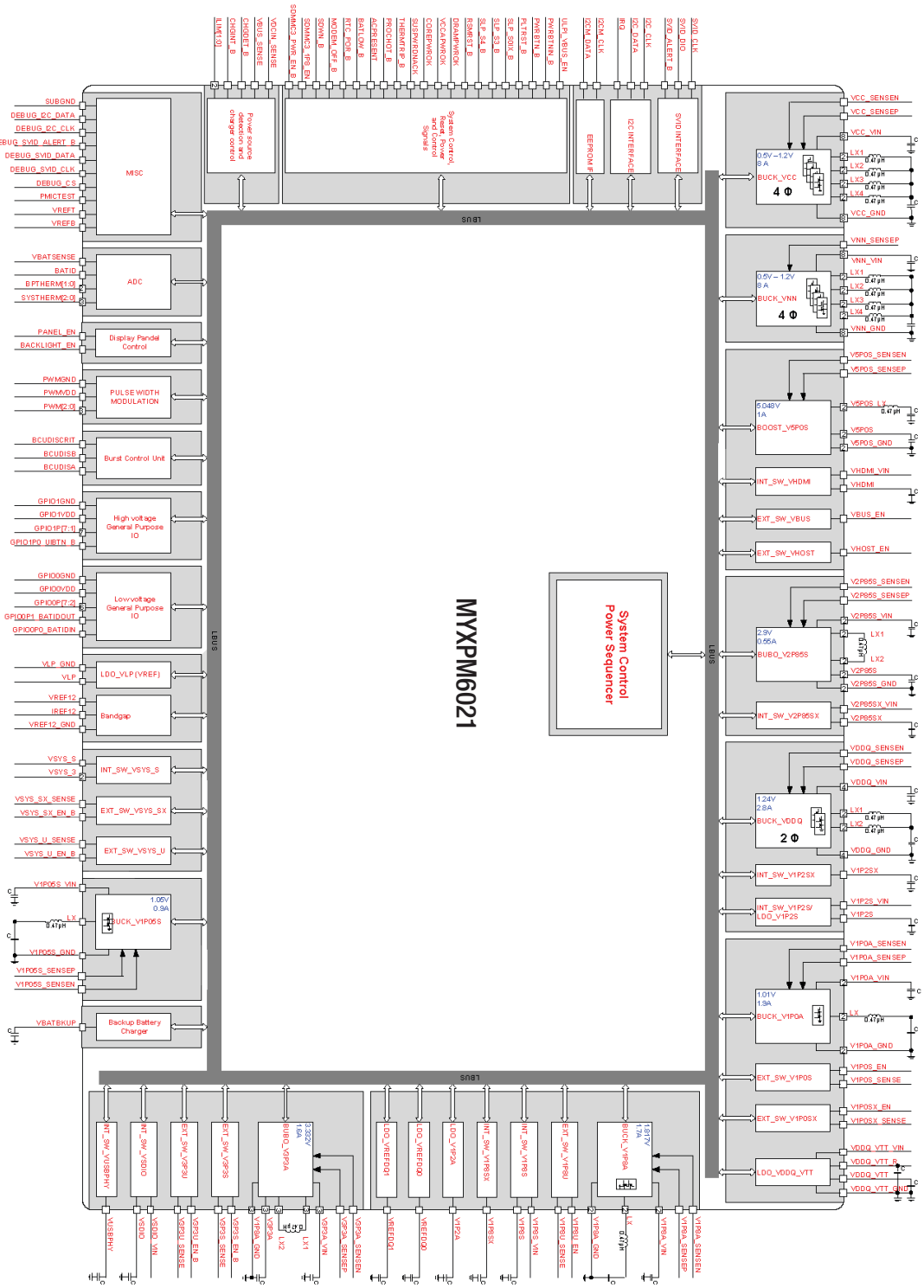
Figure 2: Detailed Block Diagram



5 Operating Conditions

All voltages are referenced to VSS unless otherwise stated. Currents flowing into MYXPM6021 are deemed positive, currents flowing out are deemed negative.

All parameters are valid over the full operating temperature range and power supply range unless otherwise noted. Please note that the power dissipation must be limited to avoid overheating of MYXPM6021. The maximum power dissipation should not be reached with maximum ambient temperature.

Table 1: Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Unit	Val
Storage Temperature	TSTOR	-65	+150	°C	Q
Operating Temperature free-air	TAMB	-30	+85	°C	E
Power Supply Input	VSUP	-0.3	+5.5	V	E/Q
IO Input	(All unless otherwise stated)	-0.3	VSUP+0.3	V	Q
Maximum Power Dissipation	60°C ambient temperature 55mmx100mmx0.75mm PCB		2.0	W	D, E
Package Thermal Resistance			TBD	K/W	D, E
ESD CDM (Charge Device Model)	All pins unless otherwise stated.		±500	V	Q
ESD HBM (Human Body Model)	All pins unless otherwise stated.		±2	kV	Q

Table 2: Recommended Operating Conditions

Parameter	Conditions	Min	Max	Unit	Val
Operating Temperature Free-Air	TAMB	-30	+85	°C	E,Q
Power Supply Input	VSUP	2.7	4.5	V	E,Q

The maximum allowed operational die temperature is 125°C. Below you can find the time constraints in relation to the peak power dissipation. The simulation results are based on:

- 10 layer board, 70x170x0.8mm3
- Natural convection, air velocity 0m/s
- Surface-to-surface radiation
- Package initializes at 0.25W with initial temperature of 38°C
- Surrounding ambient temperature in immediate vicinity at 31°C
- Maximum power burst exposure of 100s

Various power burst scenarios at: 0.76, 0.96, 1.20, 2.90, 3.72, 4.52 and 7.0W

6 Pinning Information

The "_B" symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage level (active low). When the "_B" is not present after the signal name the signal is asserted when the signal is at a high voltage level.

Table 3: Pin Description

	Pin Name	Pins	Power Domain	Description	Type
VCC	VCC_VIN	8	VSYS	VCC buck input supply	IP
	VCC_GND	8	GND	VCC buck ground	IP
	VCC_LX	8	VSYS	Quad phase switching nodes	OP
	VCC_FBP	1	VCC	VCC feedback positive sense	IA
	VCC_FBN	1	VCC	VCC feedback ground sense	IA
VNN	VNN_VIN	8	VSYS	VNN buck input supply	IP
	VNN_GND	8	GND	VNN buck ground	IP
	VNN_LX	8	VSYS	Quad phase switching nodes	OP
	VNN_FBP	1	VNN	VCC feedback positive sense	IA
V1P0A	V1P0A_VIN	2	VSYS	V1P0A buck input supply	IP
	V1P0A_GND	2	GND	V1P0A buck ground	IP
	V1P0A_LX	2	VSYS	V1P0A phase switching nodes	OP
	V1P0A_FBP	1	V1P0A	VCC feedback positive sense	IA
	V1P0A_FBN	1	V1P0A	VCC feedback negative sense	IA
V1P05S	V1P05S_VIN	1	VSYS	V1P05S buck input supply	IP
	V1P05S_GND	1	GND	V1P05S buck ground	IP
	V1P05S_LX	1	VSYS	V1P05S phase switching nodes	OP
	V1P05S_FBP	1	V1P05S	V1P05S feedback sense pos	IA
	V1P05S_FBN	1	V1P05S	V1P05S feedback sense neg	IA
VDDQ	VDDQ_VIN	4	VSYS	VDDQ buck input supply	IP
	VDDQ_GND	4	GND	VDDQ buck ground	IP
	VDDQ_LX	4	VSYS	VDDQ phase switching nodes	OP
	VDDQ_FBP	1	VDDQ	VDDQ feedback positive sense	IA
	VDDQ_FBN	1	VDDQ	VDDQ feedback negative sense	IA

Table 3: Pin Description (continued)

	Pin Name	Pins	Power Domain	Description	Type
V1P8A	V1P8A_VIN	2	VSYS	V1P8A buck input supply	IP
	V1P8A_GND	2	GND	V1P8A buck ground	IP
	V1P8A_LX	2	VSYS	V1P8A phase switching nodes	OP
	V1P8A_FBP	1	V1P8A	V1P8A feedback positive sense	IA
	V1P8A_FBN	1	V1P8A	V1P8A feedback negative sense	IA
V3P3A	V3P3A_VIN	3	VSYS	V3P3A buck boost input supply	IP
	V3P3A_GND	3	GND	V3P3A buck boost ground	IP
	V3P3A_LX1	3	VSYS	V3P3A LX node 1	IA
	V3P3A_LX2	3	VSYS	V3P3A LX node 2	IA
	V3P3A	3	V3P3A	V3P3A output	OP
	V3P3A_FBP	1	V3P3A	V3P3A feedback positive sense	IA
	V3P3A_FBN	1	V3P3A	V3P3A feedback ground sense	IA
V2P85S	V2P85S_VIN	2	VSYS	V2P85S buck boost input supply	IP
	V2P85S_GND	2	GND	V2P85S buck boost ground	IP
	V2P85S_LX1	2	VSYS	V2P85S LX node 1	IA
	V2P85S_LX2	2	VSYS	V2P85S LX node 2	IA
	V2P85S	2	V2P85S	V2P85S output	OP
	V2P85S_FBP	1	V2P85S	V2P85S feedback positive sense	IA
	V2P85S_FBN	1	V2P85S	V2P85S feedback ground sense	IA
V5P0S	V5P0S_GND	2	GND	V5P0S buck boost ground	IP
	V5P0S_LX	2	VSYS	V5P0S LX node 1	IA
	V5P0S	2	V5P0S	V5P0S output	OP
	V5P0S_FBP	1	V5P0S	V5P0S feedback positive sense	IA
	V5P0S_FBN	1	V5P0S	V5P0S feedback positive sense	IA
VDDQ_VTT	VDDQ_VTT_VIN	1	V1P0A	VDDQ_VTT input voltage	IP
	VDDQ_VTT_GND	1	GND	VDDQ_VTT ground	IP
	VDDQ_VTT	1	VDDQ_VTT	VDDQ_VTT output voltage	OP
	VDDQ_VTT_R	1	VDDQ_VTT	VDDQ_VTT reference voltage	OP
V1P8U	V1P8U_EN_B	1	V1P8A	V1P8U enable signal	OD
	V1P8U_FB	1	V1P8U	V1P8U sense line	IA

Table 3: Pin Description (continued)

	Pin Name	Pins	Power Domain	Description	Type
V1P8S	V1P8S_VIN	1	V1P8A	V1P8S input voltage	IP
	V1P8S	1	V1P8S	V1P8S output voltage	OP
V1P8SX	V1P8SX	1	V1P8SX	V1P8SX V1P8SX output voltage	OP
V1P2S	V1P2S	1	V1P2S	V1P2S output voltage	OP
V1P2A	V1P2A	1	V1P2A	V1P2A output voltage	OP
V1P2SX	V1P2SX	1	V1P2SX	V1P2SX output voltage	OP
	V1P2SX_IN	1	V1P8A	V1P2SX input voltage	IP
VREFDQ0	VREFDQ0	1	VREFDQ0	VREFDQ0 output voltage	OP
VREFDQ1	VREFDQ1	1	VREFDQ1	VREFDQ1 output voltage	OP
V3P3U	V3P3U_EN	1	V3P3A	V3P3U input voltage	IP
	V3P3U_FB	1	V3P3U	V3P3U output voltage	OP
V3P3S	V3P3S_EN_B	1	V3P3A	V3P3U input voltage	IP
	V3P3S_FB	1	V3P3S	V3P3S sense signal	IA
VSDIO	VSDIO_VIN	1	V3.3A	VSDIO input voltage	OP
	VSDIO	1	VSDIO	VSDIO output voltage	OP
VUSBPHY	VUSBPHY	1	VUSBPHY	VUSBPHY output voltage	OP
VHOST	VHOST_EN	1	VHOST	VHOST enable signal	OD
VBUS	VBUS_EN	1	VBUS	VBUS enable signal	OD
	ULPI_VBUS_EN	1	VSYS	Input signal to enable VBUS	ID
VHDMI	VHDMI_VIN	1	VHDMI	VHDMI input voltage	IP
	VHDMI	1	VHDMI	VHDMI output voltage	OP
V2P85SX	V2P85SX_VIN	1	V2P85S	V2P85SX input voltage	IP
	V2P85SX	1	V2P85SX	V2P85SX output voltage	OP
VSYSU	VSYSU_EN	1	VSYS	VSYSU input voltage	OP
	VSYSU_FB	1	VSYSU	VSYSU output voltage	IP
VSYSS	VSYSS	1	VSYSS	VSYSS output voltage	OP
VSYS_SX	VSYS_SX_EN#	1	VSYS_SX	VSYS_SX enable signal	OD
	VSYS_SX_FB	1	VSYS_SX	VSYS_SX sense signal	IA
V1P0S	V1P0SEN	1	V1P0A	V1P0S enable signal	OD
	V1P0S_FB	1	V1P0A	V1P0S sense signal	IA

Table 3: Pin Description (continued)

	Pin Name	Pins	Power Domain	Description	Type
V1P0SX	V1P0SXEN	1	V1P0A	V1P0SX enable signal	OD
	V1P0SX_FB	1	V1P0A	V1P0SX sense signal	IA
BG	VREF12	1	VREF12	Bandgap reference voltage	OP
	IREF12	1	IREF12	Bandgap reference current	OP
	VREF12_QUIET	1	VSS_QUIET	Quiet ground connection	IP
VLP	VLP	1	VLP	VLP output voltage	OP
	VLP_GND	1	VLP_GND	VLP ground	IP
VSYS1/2	VSYS	2	VSYS	MYXPM6021 input supply voltage	IP
SVID	SVID_CLK	1	V1P0S	Serial VID clock signal	ID
	SVID_DIO	1	V1P0S	Serial VID data in/out	IOD
	SVID_ALERT_B	1	V1P0S	Serial VID to SoC interrupt	OD
Power Source Detection & Charger Control	VDCIN_SENSE	1	5V	AC/DC adapter input voltage detection (20V via ext. components)	IP
	ACPRESENT	1	V1P8	Valid AC/DC adapter voltage detection	OD
	VBUSSENSE	1	VUSBPHY	USB input voltage detection (20V via ext. components)	IP
	CHGDET_B	1	VSYS	USB DCP detection from USBPHY (0=USB DCP)	ID
	CHGRINT_B	1		Battery charging status 0=charging in progress 1=charging complete	IA
	ILIM[1:0]	2	VSYS	Charging current limit	OD
System Control	I2C_CLK	1	V1P8S	I2C clock signal	ID
	I2C_DATA	1	V1P8S	I2C data IO	IOD
	IRQ	1	V1P8S	Interrupt signal to So	OD
	I2CM_CLK	1	VSYS	I2C clock signal	OD
	I2CM_DATA	1	VSYS	I2C data IO	IOD
	PWRBTNIN_B	1	VSYS	System power button input	ID
	PWRBTN	1	V1P8A	System power button output	OD
	PLTRST_B	1	V1P8A	Platform reset signal	OD
	SLP_S0iX_B	1	V1P8A	Standby S0iXtrigger 0=enter S0iX 1=exit S0iX	ID

Table 3: Pin Description (continued)

	Pin Name	Pins	Power Domain	Description	Type
System Control	SLP_S3_B	1	V1P8A	Sleep S3 trigger 0=enter S3 1=exit S3	ID
	SLP_S4_B	1	V1P8A	Sleep S4 trigger 0=enter S4 1=exit S4	ID
	RSMRST_B	1	V3P3A	Resume reset to SoC, deassertion (=1) after V3P3A	OD
	DRAMPWROK	1	VDDQ	Asserted after VDDQ stable	OD
	VCCAPWROK	1	VDDQ	Power good indication to SoC	OD
	COREPWROK	1	V3P3A	Power good indication to SoC	OD
	SUSPWRDNACK	1	V1P8A	Power off indication for _A power rails	ID
	BATLOW_B	1	V1P8A	Indicating that battery voltage is not high enough to boot	OD
	THERMTRIP_B	1	V1P8S	Catastrophic thermal event, shut down all power rails	ID
	PROCHOT_B	1	V1P0S	Open drain output to SoC indicating to limit the power	OD
	SDMMC3_1P8_EN	1	V1P8S	1.8/3.3V selection for SD card 0=3.3V 1=1.8V	ID
	SDMMC3_PWR_EN_B	1	V1P8S	SD card power enable 1=off	ID
	MODEM_OFF_B	1	V1P8A	Modem reset signal	OD
	SDWN_B	1	V1P8A	System shut down warning or SIM card removal	OD
	RTCPOR	1	VRTC	Power on reset from system to PMIC	ID
Low Voltage GPIOs	GPIO0P0_BATIDIN	1	GPIO0VDD		IOD
	GPIO0P1_BATIDOUT	1	GPIO0VDD		IOD
	GPIO0P[7:2]	6	GPIO0VDD		IOD
	GPIO0VDD	1	V1P8A	Low voltage GPIO supply	IP
	GPIO0GND	1	GND	Low voltage GPIO ground	IP

Table 3: Pin Description (continued)

	Pin Name	Pins	Power Domain	Description	Type
High Voltage GPIOs	GPIO1P0_UIBTN_B	1	GPIO1VDD		IOD
	GPIO1P[7:1]	7	GPIO1VDD		IOD
	GPIO1VDD	1	V3P3A/VSYS	High voltage GPIO supply	IP
	GPIO1GND	1	GND	High voltage GPIO ground	IP
Burst Control Unit	BCUDISA	1	V1P8A	BCU warning zone A output disable signal	OD
	BCUDISB	1	V1P8A	BCU warning zone B output disable signal	OD
	BCUDISCRIT	1	V1P8A	BCU critical zone output disable signal	OD
PWM	PWM[2:0]	3	PWMVDD	PWM output signals	OD
	PWMVDD	1	V1P8A	PWM supply voltage	IP
	PWMGND	1	GND	PWM ground	IP
Display	BACKLIGHT_EN	1	V3P3A	Backlight enable	OD
	PANEL_EN	1	V3P3A	LCD panel enable	OD
ADC	SYSTHERM[2:0]	3	VLP	System temperature thermistor input	IA
	BPTHERM0	1	VLP	Battery temperature input of pack 0	IA
	BPTHERM1	1	VLP	Battery temperature input of pack 1	IA
	BATID	1	VLP	Battery identification	IA
	VBATSENSE	1	VBAT	Battery sense voltage	IA
Test	PMICTEST	1	5V	Test pin	IA
	VBATBKUP	1		Coin Cell backup battery	OP
	VREFB	1	VLP	Battery ID bias voltage	OP
	VREFT	1	VLP	Battery thermistor bias voltage	OP
	DEBUG_CS	1	VSYS	Selecting SVID and I2C channel for debugging	I
	DEBUG_SVID_CLK	1	V1P0S	SVID clock from Valleyview 2 debug channel	I
	DEBUG_SVID_DATA	1	V1P0S	SVID data in/out, debug channel	IO
	DEBUG_SVID_ALERT_B	1	V1P0S	SVID interrupt from PMIC debug channel	O

Table 3: Pin Description (continued)

	Pin Name	Pins	Power Domain	Description	Type
	DEBUG_I2C_CLK	1	V1P8S	I2C clock debug channel	I
	DEBUG_I2C_DATA	1	V1P8A	I2C data debug channel	IO

Table 4: Pin Type Definition

Pin Type	Description	Pin Type	Description
I	Input	D	Digital
O	Output		
P	Power		
A	Analog		

7 Operating Conditions

7.1 System Control Signals

7.1.1 VDCIN_SENSE

Input voltage is limited to the maximum input voltage via the resistor divider of the AC/DC adapter.

7.1.2 ACPRESENT

ACPRESENT is an active high dedicated output signal that indicates the AC/DC adapter or USB DCP/CDP/ACA (CHGDET_B=0) is connected to a valid voltage.

7.1.3 VBUS_SENSE

USB input voltage detection.

7.1.4 CHGDET_B

USB DCP detection from USBPHY to MYXPM6021. (0=USB DCP/CDP/ACA).

7.1.5 VSYS1/2

Input power supplies and input voltage supervision.

7.1.6 CHGSTAT

Input to MYXPM6021 indicating the battery charger status and fault indicator from charger IC.

7.1.7 ILIM[1:0]

Output signals providing information the external connected power sources like AC adapter, USB DCP/CDP/ACA and USB SDP).

7.1.8 I2C_CLK

I2C clock signal from SoC to MYXPM6021.

7.1.9 I2C_DATA

I2C data connection between SoC and MYXPM6021.

7.1.10 IRQ

IRQ is an active high dedicated output signal that generates interrupts to the SOC. It is asserted when at least one unmasked interrupt bit is set in the 1st level interrupt register. It is valid when RSMRST_B=1 (de-asserted). The maximum latency from the IRQ detection to the assertion of the IRQ line is 1ms.

7.1.11 I2CM_CLK

I2C clock signal from MYXPM6021 to external I2C EEPROM.

7.1.12 I2CM_DATA

I2C data line between MYXPM6021 and external I2C EEPROM.

7.1.13 PWRBTNIN_B

System power button input signal, which is internally connected to VSYS via a 20kΩ resistor. It includes a 30ms debouncer from proper function which avoids detection during bouncing contacts.

7.1.14 PWRBTN_B

MYXPM6021 passes the power button input information via the PWRBTN_B output signal to the SOC. PWRBTN_B is a level shifted copy of PWRBTNIN_B after the 30ms de-bouncer. PWRBTN_B is valid when RSMRST_B=1 (deasserted).

7.1.15 PLTRST_B

PLTRST_B is an active low dedicated input signal from the SOC that indicates the SOC already comes out of reset upon de-assertion (PLTRST_B=1). Please note that PLTRST_B is not a power state indication signal while SLP_S*_B (i.e. SLP_S0IX_B or SLP_S3_B or SLP_S4_B) signals are. PMIC ignores the PLTRST_B if it is in one of the standby states.

7.1.16 SLP_S0iX_B

SLP_S0IX_B is an active low dedicated input signal from the SOC that indicates SX state entry upon assertion (SLP_S0IX=LOW) and exit upon de-assertion (SLP_S0IX=HIGH). The assertion of the SLP_S0IX_B signal from the SOC launches SOC_SX entry sequence. It is only considered if RSMRST_B=1.

7.1.17 SLP_S3_B

SLP_ S3_B is an active low dedicated input signal from the SOC that indicates S3 state entry upon assertion (SLP_S3_B=LOW) and exit upon de-assertion (SLP_ S3_B=HIGH). The assertion/de-assertion of the SLP_S3_B signal from the SOC launches SOC_S3 state entry/exit sequence. It is valid when RSMRST_B=1 (de-asserted).

7.1.18 SLP_S4_B

SLP_S4_B is an active low dedicated input signal from the SOC that indicates S4 state entry upon assertion (SLP_S4_B=LOW) and exit upon de-assertion (SLP_S4_B=HIGH). The assertion/de-assertion of the SLP_S4_B signal from the SOC launches SOC_S4 state entry/exit sequence. It is valid only when RSMRST_B=1.

7.1.19 RSMRST_B

RSMRST_B is an active low dedicated output signal. RSMRST_B asserts when voltage rail V3P3A is enabled. RSMRST_B shall be actively driven to low in SOC G3 state when SUS rails are turned off. This is down via a pull-down integrated resistor. The nominal voltage of RSMRST_B is 0V when asserted, 3.3V when de-asserted.

7.1.20 DRAMPWROK

DRAMPWROK is an active high dedicated output signal. DRAMPWROK asserts when voltage rail VDDQ is enabled. The nominal voltage of DRAMPWROK is VDDQ when asserted, 0V when de-asserted.

7.1.21 VCCAPWROK

VCCAPWROK is an active high dedicated output signal. VCCAPWROK asserts when all voltage rails that are supposed to be on in SOC_S0 and SOC_SX states are at nominal voltage. The nominal voltage of VCCAPWROK is VDDQ when asserted, 0V when de-asserted. VCCAPWROK will de-assert only if both PLTRST_B and SLP_S0IX_B are asserted (=0) during sleep state entry.

7.1.22 COREPWROK

COREPWROK is an active high dedicated output signal. COREPWROK asserts when all voltage rails that are supposed to be on in SOC_S0 and SOC_SX states, are at nominal voltage. COREPOWROK shall be actively driven to low in SOC G3 state when SUS rails (*_A rails) are turned off. The nominal voltage of COREPWROK is 3.3V when asserted, 0V when de-asserted. COREPWROK will de-assert only if both PLTRST_B and SLP_S0IX_B are asserted (=0) during sleep state entry.

7.1.23 SUSPWRDNOK

SUSPWRDNACK is an active high dedicated input signal from the SOC that indicates the PMIC to turn off the SUS rails (A) rails (V3P3A, V1P8A, V1P0A) in junction with assertion of SLP_S4_B. It is valid when RSMRST_B=1 (de-asserted) and SLP=S4_B=0 (asserted).

7.1.24 BATLOW_B

BATLOW_B is an active low dedicated output signal to the SOC indicating that the battery voltage is not sufficiently high to boot the SoC.

7.1.25 SUSCLK

SUSCLK is the 32.768kHz RTC clock that is supplied from the SoC. It is available to MYXPM6021 about 100ms after RSMRST_B is de-asserted and continue to be available in S0, S0iX, S3 and S4 state. It is not available if the platform will be in G3 mode when the suspend voltage rails are disabled.

7.1.26 THERMTRIP_B

THERMTRIP_B is an active low dedicated input signal that notifies the PMIC of a SOC thermal event. It is valid when RSMRST_B=1 and PLTRST_B=1 (de-asserted). Upon sensing the THERMTRIP_B signal has transitioned low, the PMIC shuts down all rails immediately (hard shutdown, not waiting for SLP_S*_B signals from the SOC to execute a Cold Off power down sequence). To avoid spurious detection during power sequencing, the THERMTRIP_B signal is only sampled if PLTRST_B is de-asserted. THERMTRIP has internal pull-up.

7.1.27 PROCHOT_B

PROCHOT_B is an active low dedicated output signal used to notify the SoC of a PMIC, battery or system thermal event. PROCHOT_B will be asserted when the PMIC temperature, battery temperature or system temperature has crossed the alert thresholds define in the thermal monitoring section. It will also assert when battery voltage drops to the threshold set in SVTM. PROCHOT_B is asserted if the PMIC die temperature rises above the internally set alert threshold, for example 110°C, to prevent the PMIC from reaching critical temperature. It is valid when RSMRST_B=1 and PLTRST_B=1 (de-asserted). The SOC will go into a lower power state until the PMIC thermal event is cleared and the pin is de-asserted. PROCHOT_B has internal pullup.

7.1.28 SDMMC3_1P8_EN

SDMMC3_1P8_EN is a dedicated input signal from the SOC to select 1.8V or 3.3V for SD card.

- SDMMC3_1P8_EN=1 to select 1.8V for SD card.
- SDMMC3_1P8_EN=0 to select 3.3V for SD card.

It is valid when RSMRST_B=1 (de-asserted) and COREPWROK=1 (asserted).

7.1.29 SDMMC3_PWR_EN_B

SDMM3_PWR_EN_B is an active low dedicated output signal to enable SD card power. It is valid when RSMRST_B=1 (de-asserted) and COREPWROK=1 (asserted).

7.1.30 MODEM_OFF_B

7.1.31 SDWN_B

The SDWN_B (Shut-Down Warning) signal is sent by the PMIC to the modem as a warning that a system shutdown event is about to take place. The SDWN_B signal is asserted (set low) during power down Task Lists. If the PMIC enters a

catastrophic shutdown condition which would normally bypass a Cold Off Task List being run, the SDWN_B pin must be asserted a minimum of 900us prior to this catastrophic shutdown commencing. The nominal voltage of SDWN_B is 0V when asserted, 1.8V when de-asserted.

7.1.32 USBRST_B

USBRST_B is an active low dedicated output signal to reset the USB PHY. The minimum pulse is 100µs when asserted. The nominal voltage of USBRST_B is 0V when asserted, 1.8V when de-asserted.

7.1.33 GPIOs

7.1.33.1 Low Voltage GPIOs

GPIO0P1_BATIDIN:

Battery ID input signal from SOC for digital battery communication. Optional function multiplexed with low voltage GPIO0P1.

GPIO0P2_BATIDOUT:

Battery ID output to SoC for digital battery communication. Optional function multiplexed with low voltageGPIO0P2.

GPIO0P[7:3]:

Low voltage GPIOs with no alternate functions.

7.1.33.2 High Voltage GPIOs

GPIO1P0_UIBTN_B:

The UIBTN_B pin is an input from a platform-defined functional interface button, such as the home button. It includes a 30ms de-bouncer to ensure that spurious transitions aren‘t logged while the switch contacts bounce on initial contact. The output of the de-bouncer enters the edge detect circuits.

GPIO1P[7:1]:

High voltage GPIOs with no alternate functions.

7.1.34 Burst Control Unit

7.1.34.1 BCUDISA

Burst controller unit warning zone A. Output signal to disable peripherals (functions).

7.1.34.2 BCUDISB

Burst controller unit warning zone B. output signal to disable peripherals (functions).

7.1.34.3 BCUDISCRIT

Burst controller unit critical zone. Output signal to disable peripherals (functions).

7.1.35 PWM[2:0]

Pulse width modulated output control signals.

7.1.36 DISPLAY

7.1.36.1 BACKLIGHT_EN

Output signal to control the display backlight.

7.1.36.2 PANEL_EN

Output signal to enable the display.

7.1.37 ADC

7.1.37.1 SYSTHERM[2:0]

System temperature thermistor input signal to be multiplexed to MYXPM6021 ADC.

7.1.37.2 BPTHERM[1:0]

Battery pack temperature input signal to be multiplexed to MYXPM6021 ADC.

7.1.37.3 BATID

Battery identification from the battery for battery presence detection and battery size indication.

7.1.37.4 VBATSENSE

Battery voltage sense input.

7.1.38 Power Button

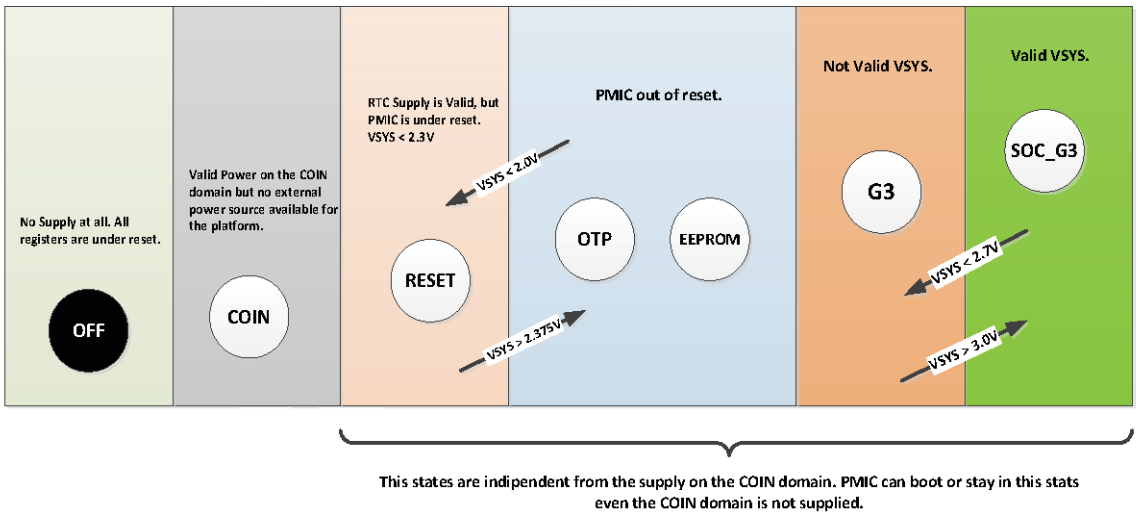
MYXPM6021 provides two buttons that can be used together to trigger the system to power on or off in different ways. Power States.

7.2 MYXPM6021 Power States

Following is a brief description of these states:

- OFF: No power at all. The platform coin cell has no valid power.
- COIN: COIN domain is powered and not under reset. Coin domain refers to a small logic portion inside MYXPM6021, which gets a reset signal and supply from the coin cell or a supercap. These logic registers retain data when MYXPM6021 supply fails or PMIC goes under the POR. These register are sitting on the analog side. The COIN state is not related to any operation in the PMIC and is not coded. It represents just a possible supply scenario.
- RESET: The digital core which is not supplied from the COIN is under POR due to the fact that the VSYS input has not crossed yet the POR release threshold.
- OTP: Just after POR is released MYXPM6021 goes into OTP state and reads the OTP. In this state all the trimming, calibration, power sequencing, and platform variant data is read and copied into the operational registers. This state is crossed only during first power up or when MYXPM6021 is forced by POR or soft reset to go back into RESET state.
- EEPROM: For debugging purpose or as a fallback solution in the field it's possible to overwrite the operational registers via an external EEPROM. This step is always performed from MYXPM6021 after the OTP state and is done once during first power up if the EEPROM contains. It is assumed that the EEPROM is supplied at the time of the access.
- G3: This state corresponds to a non-valid system supply VSYS (VSYS < VSYSREF = 3.0V). VSYS is not considered to be good enough for booting.
- SOC_G3: This is by definition the "system power down" state. Application will be mainly looping between active state and this state. VSYS valid event makes the PMIC going from G3 to SOC_G3 state. Critical events and power button can lead the PMIC to this state. Only in this state it is possible to be sensitive to the external wakeup events.

Figure 3: MYXPM6021 power up states

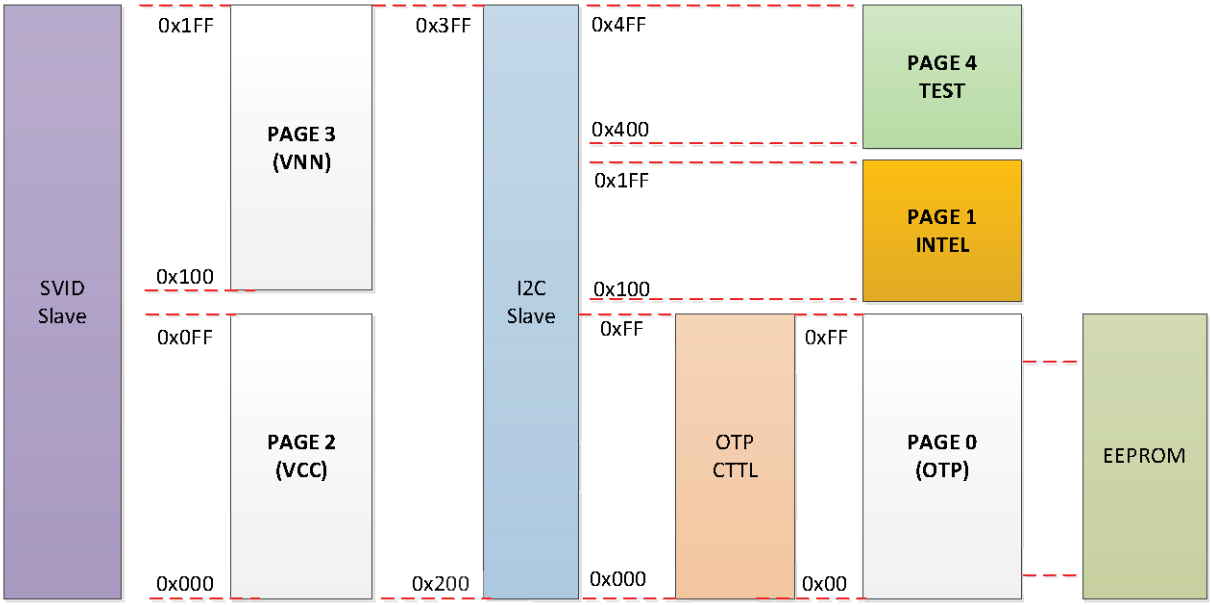


MYXPM6021 will issue an under voltage flag when VSYS will fall below the 2.7V threshold. In this case a shutdown will be executed bringing down all rails in an ordered fashion. The final state will be G3.

7.3 Register File and Address Range

There are 5 register blocks, one for VNN, one for VCC, one for test purpose, one for Intel and another block controlling the power sequence. These blocks can either be accessed via the SVID or I2C interface, via OTP or the external EEPROM, see picture blow.

Figure 4: Address Range and Pages



The power sequence is located in the page 0 of the register map and shall not be modified by customer. It is highly recommended not to modify any register in page 0 as this may damage the system. Please contact Micross if you need changes in the sequencing. Such updates can be made in 2 ways, via new OTP, This would mean producing a new MYXPM6021 variant, or via an external EEPROM.

Page 1 includes all the registers to control the ADC functions, GPIO's, PWM controller, controllable voltage domains and further functions described in the document below.

Page 2 and 3 include the SVID functions for the core and the graphics regulators.

Page 4 is an internal register block for MYXPM6021 internal test functions.

8 Power Controller State Machine

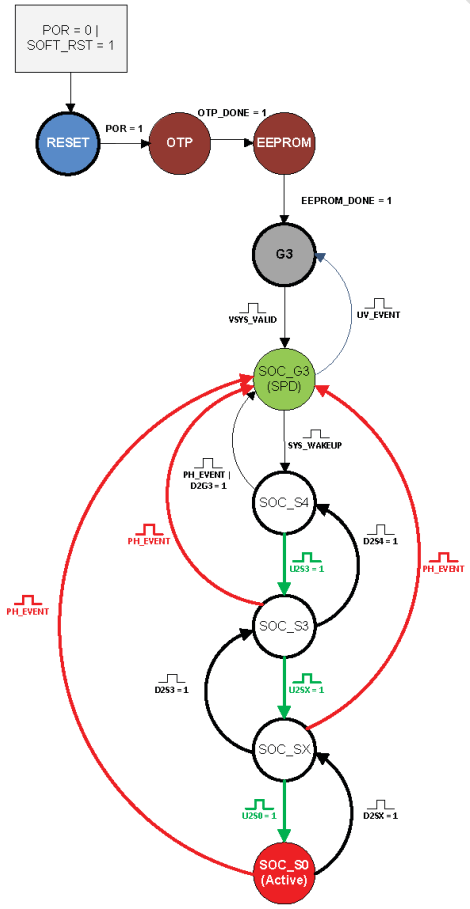
8.1 Overview

The power controller state machine is the main state machine of the MYXPM6021. It is comprised of two phases. The first phase impliments the power up sequence. It evaluates all of the conditions for a safe boot up and the configuration data is also read out of the OTP/EEPROM. The second phase impliments the power sequencing so that all of the power rails for the SoC and the platform are turned on according to certain sequencing rules.

The sequencer is very flexible in terms of component enable ordering and the intermediate delays between them. Optionally the sequencer can wait for a certain condition; for example a breakpoint, an external programmed trigger or waiting in a system power state like SOC_S4. The sequence configuration is stored in the OTP memory, the contents of which are read out during the first power up cycle. The sequencer also controls the clock request for different blocks.

8.2 Power State Transitions

Figure 5: State Transitions



8.2.1 Sequencing

Each PMIC component (such as a DC/DC converter, LDO, internal or external power switch …) can be configured with great flexibility to control the power sequencing, including the independent enabling and disabling of each component during power-up and power-down. The sequencing is defined by the Intel processor specification, with the implementation accordingly. Customers requesting power sequencing other than specified, should contact Micross Components.

8.3 MYXPM6021 Power Sequences

There are 10 power state transitions supported by the MYXPM6021. These are:

- Cold Boot: A cold boot sequence begins at the “SOC G3” state, and terminates at the “SOC S0” state. Once all of the rails are on, the COREPWROK signal will assert and the PLTRST_B will de-assert. This will effectively turn on the SOC in order for it to begin executing code and controlling the system.
- Warm Reset: A Warm Reset resets the SOC as well as the I2C and SVID interfaces (reset corresponding state machine, ignore any on-going transaction on the bus) in the PMIC. In addition the VCC, VNN will change the output voltage to the VBOOT settings. PMIC configuration registers are not reset to default. During a Warm Reset, only the PLTRST_B pin to the SOC is toggled. All rails remain in regulation. Warm reset can only be issued while the SoC stays in SOC_S0 state.
- Enter SOC S0iX: The S0IX state is entered when the SOC is in a shallow sleep state. This state is entered when the SOC asserts the SLP_S0IX_B (LOW) pin to the PMIC. VDDQ_VTT and SX rails are turned off. The VCC rail is turned off by SVID commands (not by SLP_S0IX_B signal). The rest of the VRs remain on but enter into power save mode.
- Exit SOCS0iX: The S0IX state is exited when the SOC de-asserts the SLP_S0IX_B pin (HIGH). VDDQ_VTT and SX rails are turned on. The VCC rail will be turned on by SVID commands (not by SLP_S0IX). The rest of the rails will come out of power save mode. Exiting the SOC_SX state will be performed within maximum 200µs.
- Enter SOC_S3: The S3 state is entered when the SOC asserts the SLP_S3_B pin (LOW). VRs that remain on enter into power save mode.
- Exit SOC_S3: The S3 state is exited when the SOC de-asserts the SLP_S3_B pin (HIGH). Voltage rails will be turned on and come out of power save mode. Exiting SOC_S3 state will be performed within 2ms maximum.
- Enter SOC_S4: The S4 state is entered when the SOC asserts the SLP_S4_B pin (LOW). VRs that remain on enter into power save mode.
- Exit SOC_S4: The S4 state is exited when the SOC de-asserts the SLP_S4_B pin (HIGH). Voltage rails will be turned on and come out of power save mode.
- Cold OFF: PMIC will go into SOC_G3 and stay until a wakeup event is not bringing it back to active state.
- Modem Reset: A Modem Reset task is initiated by setting the MODEMRSTSEQ bit in the MODEMCTRL register. (The MODEMOFF bit in the same register directly controls the status of the MODEM_OFF_B output pin, but does not launch this task). The Modem Reset task toggles the SDWN and MODEM_OFF_B pins, implementing appropriate (modem-specific) delay timings.

9 Platform Power Domains

9.1 Power Domains Summary

The power supply part of MYXPM6021 consists of various power supplies modules:

Table 5: Power Domains

Power Supply Module	MYXPM6021 Supplied Pins	Supplied Voltage	Supplied Current	Notes
BUCK_CORE	VCC	0.5 – 1.2V ±2% accuracy (DC & ripple) Default: 1.0V ±1.5%	8000mA	Quad phase buck converter, including IMVP-7 SVID interface with a voltage granularity of 10mV
BUCK_GRAPHIC	VNN	0.5 – 1.2V ±2% accuracy (DC & ripple) Default: 1.0V ±1.5%	8000mA	Quad phase buck converter, optional triple phase buck (OTP), including IMVP-7 SVID interface with a voltage granularity of 10mV
BUCK_V1P0	V1P0A	1.00V ±2% accuracy (DC & ripple)	1900mA	Single phase buck converter Nominal voltage 1.01V
BUCK_V1P05S	V1P05S	1.05V ±2% accuracy (DC & ripple)	475mA	Single phase buck converter Nominal output voltage 1.05V
BUCK_1P8	V1P8A	1.8V ±2% accuracy (DC & ripple)	1627mA	Single phase buck converter Nominal voltage 1.817V
BUCK_VDDQ	VDDQ	1.5/1.35/1.25V ±2% accuracy (DC & ripple)	2800mA	Dual phase buck converter Nominal voltage 1.24V
BUBO_V3P3	V3P3A	3.3V ±2% accuracy (DC & ripple)	1569mA	Buck boost converter Nominal voltage 3.332V
BUBO_V2P85	V2P85S	2.9V ±4% accuracy (DC & ripple & transient over/under)	550mA	Buck boost converter Nominal voltage 2.9V
BOOST_V5P0	V5P0S	5.0V ±4% accuracy (DC & ripple & transient over/under))	1000mA	Boost converter Nominal voltage 5.048V

Table 5: Power Domains (continued)

Power Supply Module	MYXPM6021 Supplied Pins	Supplied Voltage	Supplied Current	Notes
LDO_VDDQ_VTT	VDDQ_VTT	½ VDDQ ±2% accuracy (DC)	325mA	Push-pull LDO for DDR3 address line termination.
LDO_V1P2A	V1P2A	1.2V ±2% accuracy (DC)	30mA	LDO supplied by BUCK_V1P8A, low quiescent current
LDO_VREFDQ0	VREFDQ0	±3% accuracy (DC & ripple)	10mA	LDO supplied by BUCK_V1P8A
LDO_VREFDQ1	VREFDQ1	±3% accuracy (DC & ripple)	10mA	LDO supplied by BUCK_V1P8A
LDO_VLP	VLP	2.5V ±1.5% accuracy (DC)	10mA	LDO supplying the internal MYXPM6021 electronic
SD/LDO_V1P2S	V1P2S	VDDQ/V1P8	34mA	Function between switching device (SD) and LDO can be selected via device order code. SD can be used with DDR3 LP memory for all other types of memories the LDO solution is proposed
SD_V1P2SX	V1P2SX	VDDQ/V1P8	155mA	Switching device to generate V1P2SX. In case of DDR3 L memory this voltage will be 1.35V
SD_VUSBPHY	VUSBPHY	VSYS/V3P3_A	40mA	Switching device supplying the USBPHY with 3.3V. If V3P3A is switched off VUSBPHY is supplied by VSYS
SD_VSDIO	VSDIO	V1P8A/V3P3A	400mA/200mA	Switching device supplying the SDIO interface. Output voltage is controlled by digital input signals from SoC
SD_V1P8S	V1P8S	V1P8A	144mA	MYXPM6021 internal switching device supplied by V1P8A
SD_V1P8SX	V1P8SX	V1P8A	240mA	MYXPM6021 internal switching device supplied by V1P8A
SD_V2P85SX	V2P85SX	V2P85S	250mA	MYXPM6021 internal switching device supplied by V2P85S
SD_VHDMI	VHDMI	V5P0S	55mA	MYXPM6021 internal switching device supplied by V5P0S
SD_VSYS_S	VSYS_S	VSYS	10mA	MYXPM6021 internal switching device supplied by VSYS
EFS_VSYSU	VSYSU	VSYS	2750mA	External p-channel FET switched power domain supplied by VSYS

Table 5: Power Domains (continued)

Power Supply Module	MYXPM6021 Supplied Pins	Supplied Voltage	Supplied Current	Notes
EFS_VSYS_SX	VSYS_SX	VSYS	2500mA	External p-channel FET switched power domain supplied by VSYS
EFS_V3P3U	V3P3U	V3P3A	700mA	External p-channel FET switched power domain supplied by V3P3A
EFS_V3P3S	V3P3S	V3P3A	584mA	External p-channel FET switched power domain supplied by V3P3A
EFS_V1P8U	V1P8U	V1P8A	355mA	External p-channel FET switched power domain supplied by V1P8A
EFS_V1P0S	V1P0S	V1P0A	410mA	External n-channel FET switched power domain supplied by V1P0A
EFS_V1P0SX	V1P0SX	V1P0A	916mA	External n-channel FET switched power domain supplied by V1P0A
EFS_VHOST	VHOST	V5P0S	900mA	External switched power domain supplied by V5P0S
EFS_VBUS	VBUS	V5P0S	900mA	External switched power domain supplied by V5P0S

9.2 Voltage Rail ON/11.2 OFF On Various Power States

Table 6: Status Power Domains

Supply Module	Voltage Domain	S0	S0ix	S3	S4/5	G3
VLV2	VCC	On	Off	Off	Off	Off
VLV2	VNN	On	On	Off	Off	Off
VLV2	V1P0A	On	On	On	On	Off
VLV2	V1P05S	On	On	Off	Off	Off
VLV2	V1P8A	On	On	On	On	Off
VLV2/DDR3	VDDQ	On	On	On	Off	Off
VLV2, Peripherals	V3P3A	On	On	On	On	Off
Peripherals	V2P85S	On	On	Off	Off	Off
Peripherals	V5P0S	On	On	Off	Off	Off
DDR3	VDDQ_VTT	On	On	Off	Off	Off
VLV2	V1P2A	On	On	On	On	Off
	VREFDQ0	On	On	On	Off	Off

Table 6: Power Status Domains (continued)

Supply Module	Voltage Domain	S0	S0ix	S3	S4/5	G3
	VREFDQ1	On	On	On	Off	Off
MYXPM6021	VLP	On	On	On	On	Off
	V1P2S	On	On	Off	Off	Off
	V1P2SX	On	Off	Off	Off	Off
Peripherals	VUSBPHY	On	On	On	On	Off
Peripherals	VSDIO	On/Off *)[1]	On/Off *)[1]	Off	Off	Off
VLV2	V1P8S	On	On	Off	Off	Off
	V1P8SX	On/Off *)[1]	Off/Off *)[1]	Off	Off	Off
Peripherals	VHDMI	On/Off *)[1]	On/Off *)[1]	Off	Off	Off
	VSYS_S	On/Off *)[1]	On/Off *)[1]	Off	Off	Off
Peripherals	VSYSU	On/Off *)[1]	On/Off *)[1]	On/Off *)[1]	Off	Off
Peripherals	VSYS_SX	On/Off *)[1]	On/Off *)[1]	Off	Off	Off
Peripherals	V2P85SX	On/Off *)[1]	On/Off *)[1]	Off	Off	Off
Peripherals	V3P3U	On/Off *)[1]	On/Off *)[1]	On/Off *)[1]	Off	Off
VLV2	V3P3S	On	On	Off	Off	Off
Peripherals	V1P8U	On	On	On	Off	Off
VLV2	V1P0S	On	On	Off	Off	Off
VLV2	V1P0SX	On	Off	Off	Off	Off
Peripherals	VHOST	On/Off *)[1]	On/Off *)[1]	Off	Off	Off
Peripherals	VBUS	On/Off *)[1]	On/Off *)[1]	Off	Off	Off

Note:

1. *) on-demand register controlled

9.3 PMIC Current Consumption in Various States

Ta = 25°C, VSYS = 3.7V, no load

Table 7: PMIC Current Consumption

Power State	Min	Typ. [mA]	Max
SOC_S0		2.089	
SOC_S0iX		1.793	
SOC_S3		1.022	
SOC_S4		0.789	

Table 7: PMIC Current Consumption (continued)

Power State	Min	Typ. [mA]	Max
SOC_G3		0.069	
G3		0.056	

9.4 Voltage Rail Control Mechanism

Proper power-up/down sequencing is mandatory to prevent damages. There are several methods controlling the power rails.

- VCC & VNN are controlled via the SVID interface
- State transitions, SOC provides SLP_S0iX_B, SLP_S3_B and SLP_S4_B signals to MYXPM6021 controlling the related power rails
- Sequencer controlling
- Dedicated register control

9.5 SVID Interface

SOC communicates with the MYXPM6021 via the SVID interface. SVID's commands composed of 9 bits – 4 MSBs determine the address and 5 LSBs are the command bits. MYXPM6021 supports 2 SVID voltage regulators – VCC & VNN. The address for each of the voltage regulator is indicated in the table below:

Table 8: VCC & VNN Addresses

Address	Target	Description
0x00	VCC	All commands will be routed to the VCC SVID registers and MYXPM6021 will respond with the VCC status information
0x01	VNN	All commands will be routed to the VNN SVID registers and MYXPM6021 will respond with the VNN status information

9.5.1 SVID DC Electrical Parameters

The following table outlines the SVID DC electrical parameters. Note that low voltage operation is essential to avoid level converters to/from the processor. MYXPM6021 SVID buffer should take V1P0S_FB as a reference voltage for improved signal integrity at the receiver.

Table 9: SVID DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V1P0S	SVID IO voltage	0.95	1.00	1.05	V	
VIL	Input low voltage			0.45* V1P0S	V	1
VIH	Input high voltage	0.65* V1P0S			V	1
VHYS	Hysteresis voltage	0.05			V	
VOH	Output high voltage		V1P0S		V	1
RON	Buffer on resistance (data line & alert# line)	10		20	Ω	2
IL	Leakage current	-100		100	uA	3
CPAD	Pad capacitance			4.0	pF	4
VPIN	Pin capacitance			5.0	pF	

Notes:

1. V1P0S refers to instantaneous voltage at V1P0S_FB location.
2. Measured at 0.31 * V1P0S.
3. VIN between 0V and V1P0S.
4. CPAD includes die capacitance only. No package parasitic included.

Figure 6: Definition of VHYS

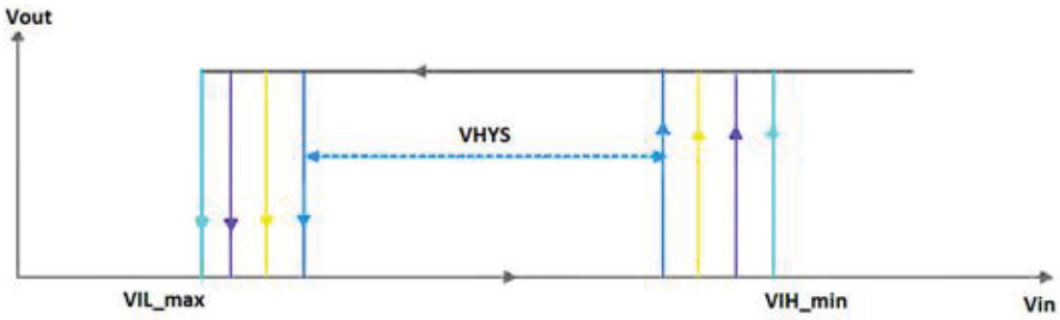


Table 10: SVID buffer AC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Vmax	VDS max open drain buffer to accommodate bus ringing	-1.00		3.30	V	
SR Fall Data/Alert		1.20		3.50	V/ns	Load: Rpu=64.9Ω
SR Rise Data/Alert		1.20		3.50	V/ns	Load: Rpu=64.9Ω

Slew Rate (SR) is measured between 0.7*V1P0S and 0.3*V1P0S. SR is measured at the output of the buffer; Rpu is connected to V1P0S as a load with no additional capacitance on the board. The slew rate is defined with VR buffer capacitance only.

9.5.2 VCLK Timing Parameters

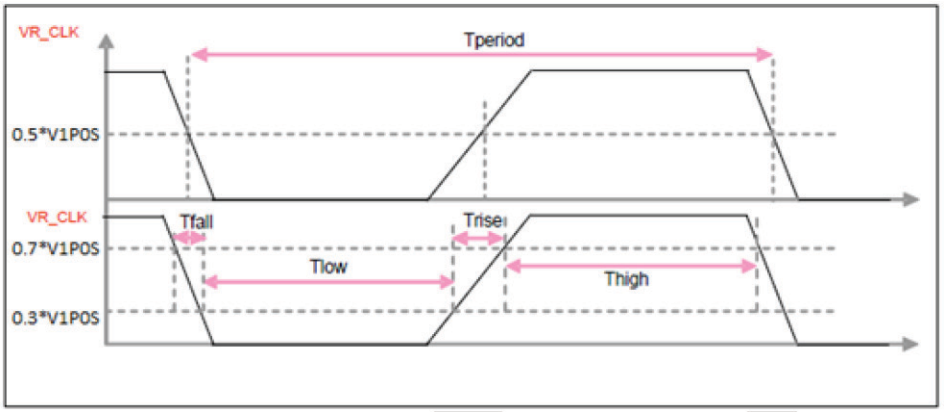
Table 11: VCLK AC Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	VCLK frequency	13.3	25	26.25	MHz	1,4
Thigh	VCLK high time	-10%		+10%	% of 0.5 Tperiod	2,4
Tlow	VCLK low time	-10%		+10%	% of 0.5 Tperiod	2,4
Trise	VCLK rise time @VR Pad	0.25		3.0	ns	3
Tfall	VCLK fall time @VR Pad	0.25		3.0	ns	3
	Duty cycle	45		55	%	1,4

Notes:

1. Period and duty cycle are measured with respect to 0.5 * V1P0S.
2. High time is measured with respect to 0.7 * V1P0S. Low time is measured with respect to 0.3 * V1P0S.
3. Rise time is measured from 0.3*V1P0S – 0.7*V1P0S. Fall time is measured 0.7*V1P0S - 0.3*V1P0S.
4. Tperiod, Thigh, Tlow and Duty Cycle variation as a result of internal CPU Clock logic only. Additional variation may be introduced as a result of the Clock MB topology (like different Rpu values or MB impedance).

Figure 7: Measurement Points for VCLK

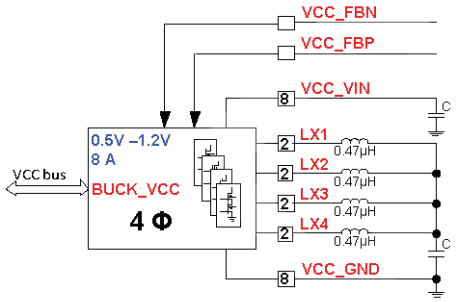


9.6 Power Supplies

9.6.1 DC/DC Buck Regulator VCC

The BUCK_CORE converter is a high efficiency synchronous quad phase step down regulator operating at a high frequency (3 MHz) supplying a voltage (VCC) of 0.5 … 1.2V at maximum 8000mA. This buck regulator has the ability to dynamically change its output voltage setting to comply with the SoC's frequency-power requirements. The output voltage is controlled using the SVID interface.

Figure 8: VCC Block Diagram



Form #: CSI-D-685 Document 011

9.6.1.1 Electrical Characteristics VCC

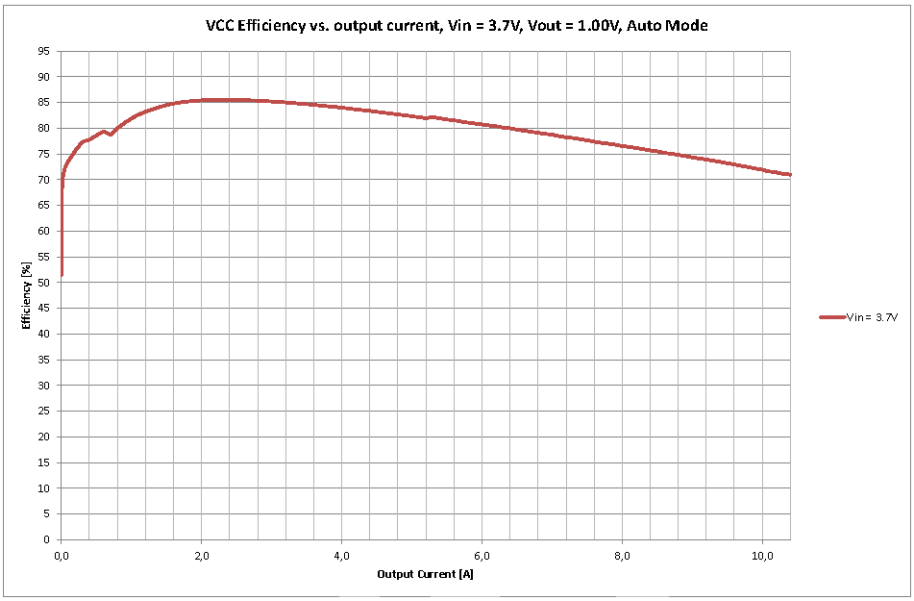
Table 12: Electrical Parameters for BUCK_VCC

Parameter	Test Conditions	Min	Typ	Max	Unit
VCC_IN Input Voltage		2.7		4.5	V
Cin at VCC_IN			4 x 4.7		µF
Cout			6 x 47		µF
ESR of output capacitor			6 @ 47µF		mΩ
ESL of output capacitor			1.6 @ 3MHz		nH
L_BUCK inductor value		-20%	4x0.47	+20%	µH
L_R inductor DC resistance				48	mΩ
VCC Output Voltage	IOUT= Imax	0.50		1.2	V
VCC Output Accuracy			See chapter 9.5.6		
F_BUCK Frequency of operation	Tablet		3		MHz
Transient load current profile	1000-8000mA 25-7000mA		200 200		ns ns
Transient droop[1]	1000-8000mA 25-7000mA			40	mV
Transient overshoot[2]	8000-1000mA 7000-25mA			40	mV
Ton Turn on time				2	ms
Toff Turn off time	Vout down to 0.5V			20	µs
Rpd Discharge impedance	0.5V down to 0V			20	Ω
IQ_ON Quiescent Current in On Mode	No load			200	µA
Normal Mode – Synchronous rectification (PWM)					
Maximum Output Current (Imax)		8000			mA
ILIMIT Current limitation	Cycle by cycle	1.3*Imax			mA
Boot up voltage for V_{CC} V_{BOOT}			1.1		V
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout	Typical BOM environment		See Figure 9		
Sleep Mode – Pulse skipping (PSK)					
Efficiency at VSYS = 3.7V & Tamb=60°C			See Figure 9		

Notes:

1. Including DC accuracy, ripple and load regulation
2. Including DC accuracy, ripple and load regulation
3. RDSON measurement on ATE

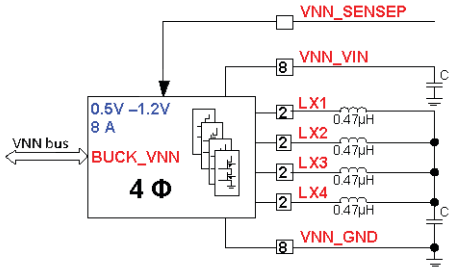
Figure 9: VCC Efficiency



9.6.2 DC/DC Buck Regulator VNN

The BUCK_VNN converter is a high efficiency synchronous step down regulator operating at a high frequency (3 MHz) supplying a voltage (VNN) of 0.5 … 1.2V at maximum 8000mA. This buck regulator has the ability to dynamically change its output voltage setting to per SoC's frequency-power requirements. The output voltage is controlled using the SVID interface.

Figure 10: Buck VNN Block Diagram



Form #: CSI-D-685 Document 011

9.6.2.2 Electrical Characteristics VNN

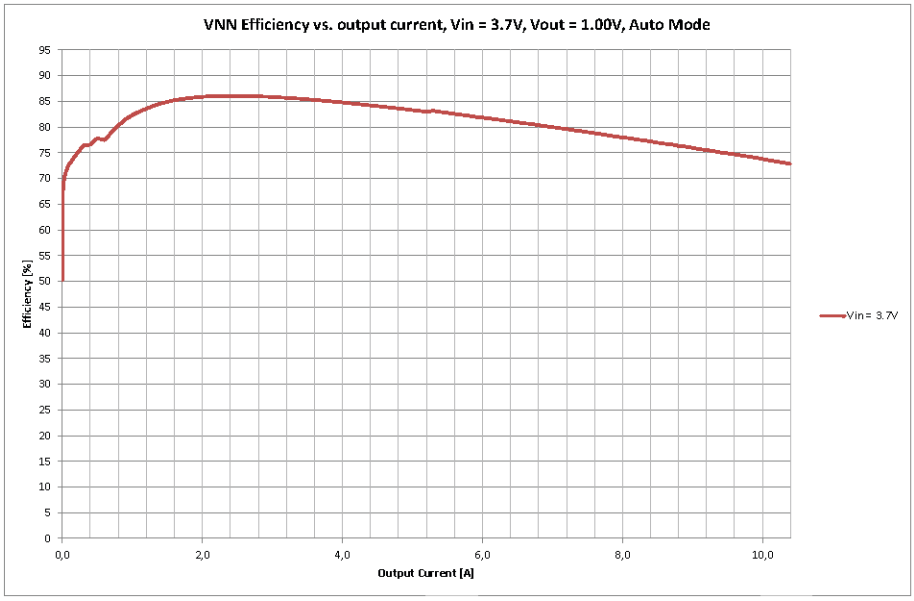
Table 13: Electrical Parameters for BUCK_VNN

Parameter	Test Conditions	Min	Typ	Max	Unit
VCC_IN Input Voltage		2.7		4.5	V
Cin at VCC_IN			4 x 4.7		µF
Cout		6 x 22			µF
ESR of output capacitor			6 @ 22µF		mΩ
ESL of output capacitor			1.6 @ 3MHz		nH
L_BUCK inductor value		-20%	4x0.47	+20%	µH
L_DCR inductor DC resistance				48	mΩ
VNN Output Voltage	IOUT= Imax	0.50		1.2	V
VNN Output Accuracy			See chapter 9.5.6		
F_BUCK Frequency of operation	Tablet		3		MHz
Transient load current profile	2900-5600mA 50-2750mA		200 200		ns ns
Transient droop[1]	2900-5600mA 50-2750mA			40	mV
Transient overshoot[2]	5600-2900mA 2750-50mA			40	mV
Ton Turn on time				2	ms
Toff Turn off time	Vout .. 0.5V			20	µs
Rpd Discharge impedance	0.5V ..0V			20	Ω
IQ_ON Quiescent Current in On Mode	No load			200	µA
Normal Mode – Synchronous rectification (PWM)					
Maximum Output Current (Imax)		8000			mA
ILIMIT Current limitation	Cycle by cycle	1.3*Imax			mA
Boot up voltage for V_{CC} V_{BOOT}			1.1		V
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout			See Figure 11		
Sleep Mode – Pulse skipping (PSK)					
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout			See Figure 11		

Notes:

1. Including DC accuracy, ripple and load regulation
2. Including DC accuracy, ripple and load regulation
3. RDSON measurement on ATE

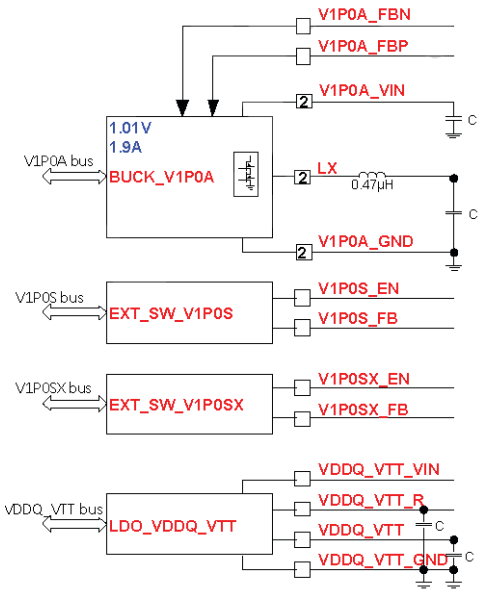
Figure 11: VNN Efficiency



9.6.3 DC/DC Buck Regulator V1P0A

The high efficiency buck regulator supplies the USB sus, clock, CFIO and the V1P0S power rails of the SoC. The power rail is also capable of supplying the pass device of the push pull source for the DDR3 address line termination.

Figure 12: V1P0A Power Rail Block Diagram



To allow for voltage drops on the PCB, it is possible to program the output voltage to either 1.01V or 1.05V. See register below.

The maximum output current of the 1P0A buck regulator is 1900mA.

9.6.3.1 Electrical Characteristics V1P0A

Table 14: Electrical Parameter for BUCK_V1P0A

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V1P0A_VIN	Input Voltage		2.7		4.5	V
Cin	At VCC_IN			2 x 4.7		µF
Cout	≥ 80µF			4 x 22 or 2 x 47		µF
ESR of output capacitor				6 @ 22/47µF		mΩ
ESL of output capacitor				1.6 @ 3MHz		nH
L_BUCK	Inductor value		-20%	0.47	+20%	µH
L_DCR	Inductor resistance				48	mΩ
V1P0A	Output voltage	IOUT= Imax	0.50		1.01 ± 2%	V
F_BUCK	Frequency of operation			3		MHz

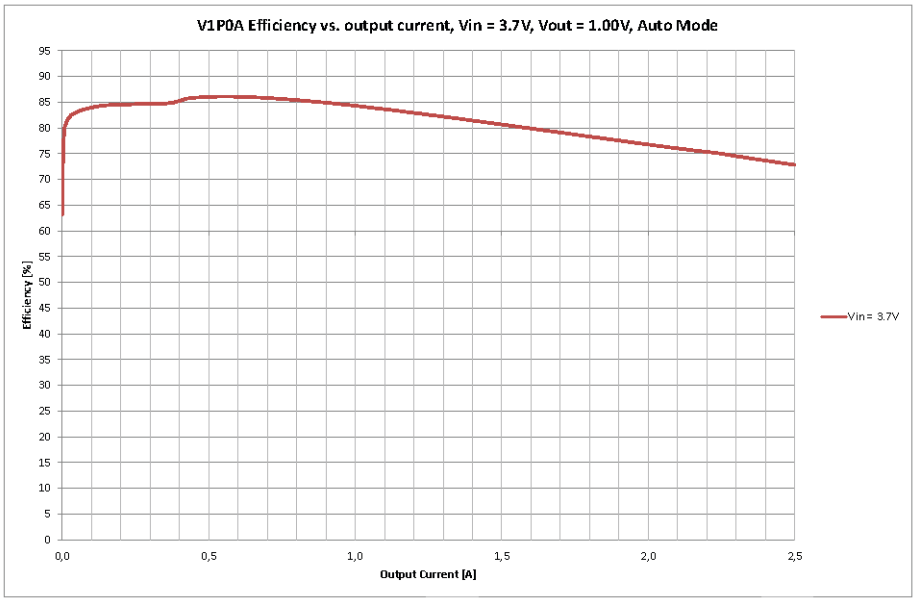
Table 14: Electrical Parameter for BUCK_V1P0A (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
Transient load current profile		5-250mA	200			ns
Transient droop[1]		75-1820mA 5-250mA			40	mV
Transient overshoot[2]		1820-75mA 250-5mA			40	mV
Ton	Turn on time				2	ms
Rpd	Discharge impedance	Vout ..0V			20	Ω
IQ_ON	Quiescent Current in On Mode	No load			50	µA
Normal Mode – Synchronous rectification (PWM)						
Maximum Output	Current (Imax)		1900			mA
ILIMIT	Current limitation	Cycle by cycle	1.3*Imax			mA
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 13		
Sleep Mode – Pulse skipping (PSK)						
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 13		

Notes:

1. Including DC accuracy, ripple and load regulation
2. Including DC accuracy, ripple and load regulation
3. RDSON measurement on ATE

Figure 13: V1P0A Efficiency



9.6.3.2 V1P0A Subsystem

V1P0S:

This voltage rail powers the SoC graphic, display & DDR3 I/O, MIPI, clock and further functions. The current requirement of this voltage rail is 410mA and requests an external switch providing this power rail to the SoC. MYXPM6021 provides a control signal named V1P0S_EN supplied by V5P0S. When this signal is asserted (high), the slew rate is controlled in order to limit the inrush current drawn via the external N-channel FET. The V1P0S_EN signal is derived from SLP_S3_B signal sent out by the SoC.

V1P0S external N-channel power switch parameters:

Rdson (Vgs=4V)	10-49mohm
Input capacitance, Ciss	700-2640pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	85-465pF

V1P0SX:

This voltage rail powers the SoC display & DDR3 I/O, PCIe and further functions. The current requirement of this voltage rail is 916mA and requests an external switch providing this power rail to the SoC. MYXPM6021 provides a control signal named V1P0SX_EN supplied by V5P0S.When this signal is asserted (high), the slew rate is controlled in order to limit the inrush current drawn via the external N-channel FET. This signal is derived from SLP_S0iX_B signal sent out by the SoC.

V1P0SX external N-channel power switch parameters:

Rdson (Vgs=4V)	10-22mohm
Input capacitance, Ciss	750-2640pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	85-465pF

VDDQ_VTT:

The VDDQ_VTT power rail is a push-pull LDO capable to source and sink maximum 325mA. VDDQ_VTT is ½ of VDDQ and its pass device is sourced by V1P0_A in order to reduce the overall power dissipation in the system.

Table 15: Electrical Parameter for VDDQ_VTT

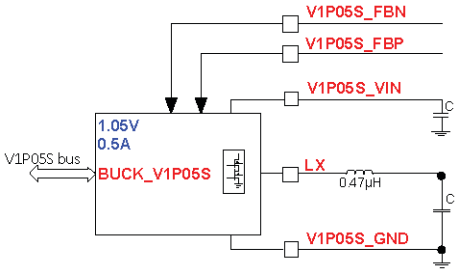
Symbol	Parameter	Min	Typ	Max	Unit	Notes / Condition
Input Requirement						
Vin (DDR3 LP)	Main input voltage VDDQ_VTT_VIN		1.01		V	Supplied by V1P0A
Vin (DDR3 L)	Main input voltage VDDQ_VTT_VIN		1.35		V	Supplied by VDDQ
Cin	VDDQ_VTT_IN		100		nF	
Output Requirement						
Vnom	Nominal output voltage		VDDQ/2		V	VDDQ used to generate VDDQ_VTT_VREF
Vtol	Output voltage tolerance	-2		+2	%	Of input supply voltage
Cout	Output capacity		10		µF	
Iout-DC	Output load current	±325			mA	
Transient load current	0-240mA	200	200		ns	
IQSC	Quiescent current VDDQ_VTT_VIN			200	µA	Iout-DC = 0mA
PSRR	Power supply rejection ratio	40	60		dB	Noise = 1 Vpp, 1-10kHz, ½ Iout-DC
Vnoise	Output Noise		60	100	µVRMS	BW = 10-100kHz, ½ Iout

9.6.4 DC/DC Buck Regulator V1P05S

This high efficiency buck regulator is the supply for the L2 SRAM of the SoC.

The maximum output current of the 1P05S buck regulator is 474mA.

Figure 14: Buck V1P05S Block Diagram



9.6.4.1 Electrical Characteristics

Table 16: Electrical Parameter for BUCK_V1P05S

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V1P05S_VIN	Input Voltage		2.7		4.5	V
Cin	At V1P05S_IN			4.7		µF
Cout				2 x 22		µF
ESR of output capacitor				6 @ 22µF		mΩ
ESL of output capacitor				1.6 @ 3MHz		nH
L_BUCK	Inductor value		-20%	0.47	+20%	µH
L_DCR	Inductor resistance				48	mΩ
V1P05S	Output voltage	IOUT= Imax		1.05±2%		V
F_BUCK	Frequency of operation			3		MHz
Transient load current profile		0-740mA		200		ns
Transient droop[1]		0-740mA			53	mV
Transient overshoot[2]		740-0mA			53	mV
Ton	Turn on time				2	ms
Rpd	Discharge impedance	Vout .. 0V			20	Ω
IQ_ON	Quiescent Current in On Mode	No load			50	µA

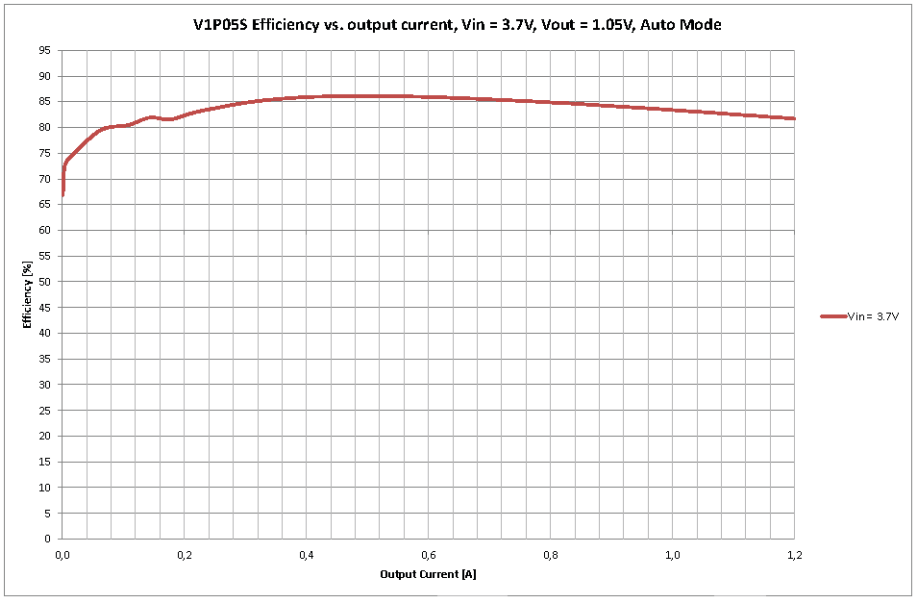
Table 16: Electrical Parameter for BUCK_V1P0A (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
Normal Mode – Synchronous Rectification (PWM)						
Maximum Output Current (Imax)			475			mA
ILIMIT	Current limitation	Cycle by cycle	900			mA
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 15		
Sleep Mode – Pulse Skipping (PSK)						
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 15		

Notes:

1. Including DC accuracy, ripple and load regulation
2. Including DC accuracy, ripple and load regulation
3. RDSON measurement on ATE

Figure 15: V1P05S Efficiency

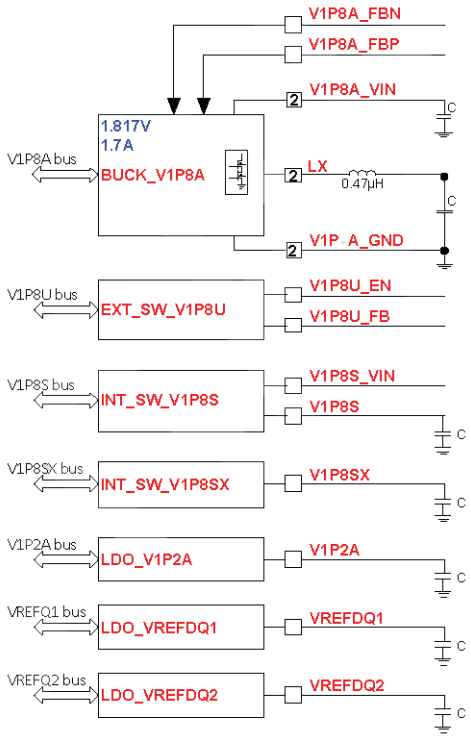


9.6.5 DC/DC Buck Regulator V1P8_A

This high efficiency buck regulator is the supply for the 1.8V I/Os, USB, V1P8U, V1P8S and V1P8SX.The maximum output current of the 1P8A buck regulator is 1627mA

9.6.5.1 Power States

Figure 16: Buck V1P8A Power Rail Block Diagram



9.6.5.2 Electrical Characteristics V1P8A

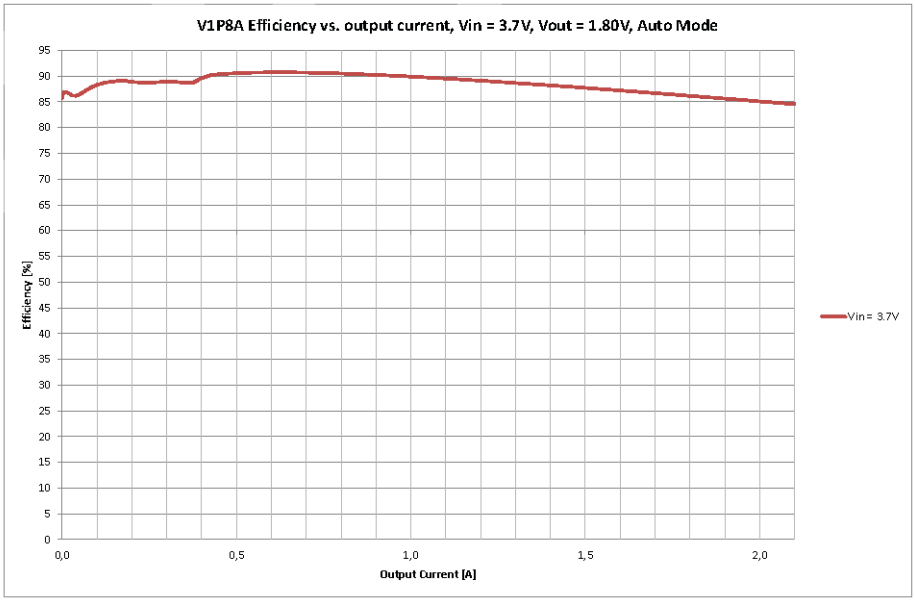
Table 17: Electrical Parameter for BUCK_V1P8A

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V1P8A_VIN	Input voltage		2.7		4.5	V
Cin	At V1P8A_IN			4.7		µF
Cout				2 x 22		µF
ESR of output capacitor				6 @ 22µF		mΩ
ESL of output capacitor				1.6 @ 3MHz		nH
L_BUCK	Inductor value		-20%	0.47	+20%	µH

Table 17: Electrical Parameter for BUCK_V1P8A (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
L_DCR	Inductor resistance				48	mΩ
V1P0A	Output v Frequency of Operation oltage	IOUT= Imax		1.817±2%		V
F_BUCK	Frequency of operation			3		MHz
Transient load current profile		0-861mA			250	ns
Transient droop[1]		0-861mA			73	mV
Transient overshoot[2]		861-0mA			73	mV
Ton	Turn on time				2	ms
Rpd	Discharge impedance	Vout .. 0V			20	Ω
IQ_ON	Quiescent current in on mode	No load			50	µA
Normal Mode – Synchronous Rectification (PWM)						
Maximum Output Current (Imax)			1627			mA
ILIMIT Current limitation		Cycle by cycle	1.3*Imax			mA
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 17		
Sleep Mode – Pulse Skipping (PSK)						
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 17		

Figure 17: V1P8A Efficiency



9.6.5.3 V1P8A Subsystems

V1P8U:

This power rail is primarily to supply LPDDR2 or LPDDR3 RAMs. MYXPM6021 provides a control signal V1P8U_EN_B supplied by VSYS and derived from SLP_S4_B sent out by the SoC. When V1P8U_EN_B is asserted low, the signal slew rate is controlled to limit the inrush current when the external P-channel FET is turned on. The current of this power rail is a maximum 355mA.

V1P8U external P-channel power switch parameters:

Rdson (Vgs=4V)	50-97mohm
Input capacitance, Ciss	750-2315pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	100-465pF

V1P8S:

The maximum current of this power rail is 145mA, sourcing the SoC, USB PHY, UICC SIM … MYXPM6021 controls this power rail while deriving the information from SoC SLP_S3_B signal and switching the rail internally. The typical RDSon value of this internal switch is 170mΩ.

Table 18: V1P8S Power Switch Specification

Description	Value [max, mΩ]
Input power path board resistance	10
Output power path board resistance	20
Input, output rails wirebond & internal FET RDS-ON	242

V1P8SX:

This power rail is used to source platform devices such as eMMC, camera, audio codecs … The maximum allowed output current is 240mA. MYXPM6021 controls this power rail while deriving the information from SoC SLP_S0ix_B signal and switching the rail internally. The typical R_{DSon} of this internal switch is 100mΩ.

Table 19: V1P8S Power Switch Specification

Description	Value [max, mΩ]
Input power path board resistance	10
Output power path board resistance	20
Input, output rails wirebond & internal FET RDS-ON	147

V1P2A:

V1P2A is a LDO that is sourced by V1P8A and generates a voltage of 1.2V to supply USB HSIC.

Table 20: Electrical Parameter for V1P2A

Symbol	Parameter	Min	Typ	Max	Unit	Notes / Condition
Input Requirement						
Vin	Main input voltage		1.80		V	Supplied by V1P8A
Output Requirement						
Vnom	Nominal output voltage		1.2		V	
Vtol	Output voltage tolerance	-2%		+2%		
Cout	Output capacity		1		µF	
Iout-DC	Output load current		1	30	mA	
IQSC	Quiescent current (operational)		10		µA	Iout-DC = 0mA
IQSC	Quiescent current (sleep)		2		µA	Iout-DC = 0mA

Table 20: Electrical Parameter for V1P2A (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes / Condition
PSRR	Power supply rejection ratio	50			dB	Noise = 0.1Vpp, 1-10kHz, ½ Iout-DC
Vnoise	Output Noise	50		100	µVRMS	10-100kHz, ½ Iout-DC

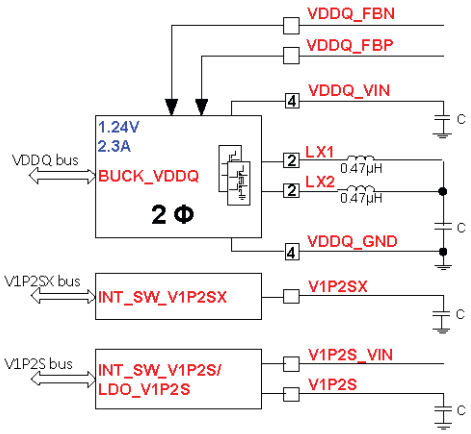
Table 21: Electrical Parameter for VREFDQ1/2

Symbol	Parameter	Min	Typ	Max	Unit	Notes / Condition
Input Requirement						
Vin	Main input voltage		1.80		V	Supplied by V1P8A
Output Requirement						
Vnom	Nominal output voltage		0.6..1.2		V	Via VREFDQ0/1_VSEL register
Vtol	Output voltage tolerance	-5%		+5%		
Cout	Output capacity		1		µF	
Iout-DC	Output load current		1	10	mA	
IQSC	Quiescent current (operational)		10		µA	Iout-DC = 0mA
IQSC	Quiescent current (sleep)		2		µA	Iout-DC = 0mA
PSRR	Power supply rejection ratio	50			dB	Noise = 0.1Vpp, 1-10kHz, ½ Iout-DC
Vnoise	Output Noise	50		100	µVRMS	10-100kHz, ½ Iout-DC

9.6.6 DC/DC Buck Regulator VDDQ

This high efficiency buck regulator is the supply for any type (1.5V/1.35V/1.25V) of DDR3 memory. The maximum output current of VDDQ buck regulator is 2800mA.

Figure 18: VDDQ Power Domain Block Diagram



9.6.6.1 Electrical Characteristics VDDQ

Table 22: Electrical Parameter for BUCK_VDDQ

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
VDDQ_VIN	Input voltage		2.7		4.5	V
Cin	At VDDQ_IN			2 x 4.7		µF
Cout				2 x 47 or 4 x 22		µF
ESR of output capacitor				6 @ 22/47µF		mΩ
ESL of output capacitor				1.6 @ 3MHz		nH
L_BUCK	Inductor value		-20%	2 x 0.47	+20%	µH
L_DCR	Inductor resistance				48	mΩ
V1P0A Output Voltage		IOUT= Imax		1.24/1.35±2%		
F_BUCK	Frequency of operation			3		MHz
Transient load current profile		35-2085mA		200		ns
Transient droop[1]		35-2085mA			50	mV
Transient overshoot[2]		2085-35mA			50	mV
Ton	Turn on time				2	ms
Rpd	Discharge impedance	VDDQ .. 0V			20	Ω
IQ_ON	Quiescent current in on mode	No load			100	µA

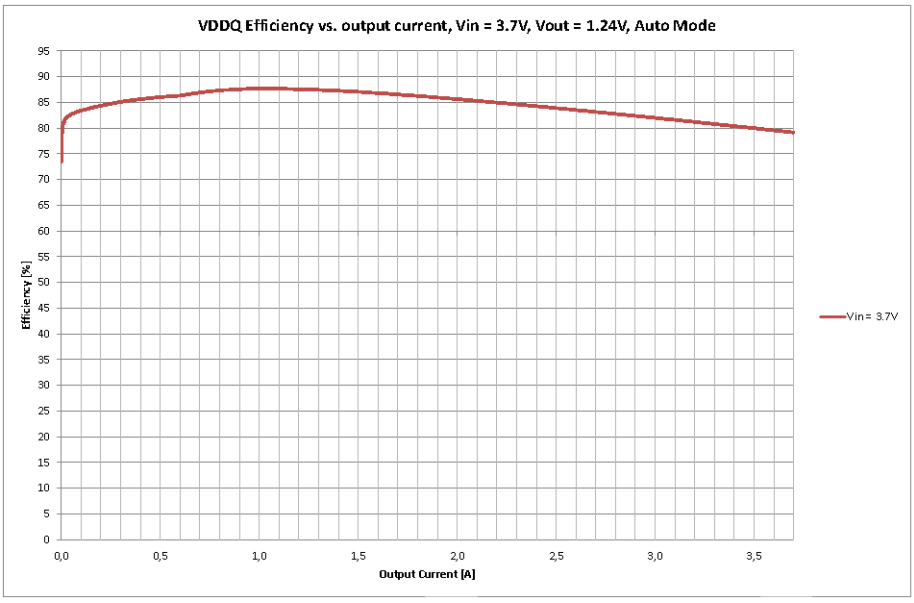
Table 22: Electrical Parameter for BUCK_V1P8A (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
Normal Mode – Synchronous Rectification (PWM)						
Maximum Output Current (Imax)			2800			mA
ILIMIT Current limitation		Cycle by cycle	1.3*Imax			mA
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 19		
Sleep Mode – Pulse Skipping (PSK)						
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 19		

Notes:

1. Including DC accuracy, ripple and load regulation
2. Including DC accuracy, ripple and load regulation
3. RDSON measurement on ATE

Figure 19: VDDQ Efficiency



9.6.6.2 VDDQ Subsystems

V1P2S:

This voltage rail is used to supply mainly the MIP interface. In case of 1.24V DDR3 memory the input voltage of this power domain is VDDQ and it acts as a power switch. For all other types of DDR3 memories the input voltage is V1P8A and V1P2S is generated via a small LDO.

Table 23: V1P2S Power Switch Specification

Description	Value [max, mΩ]
Input power path board resistance	20
Output power path board resistance	20
Input, output rails wirebond & internal FET RDS-ON	620

Table 24: Electrical Parameter for V1P2S LDO

Symbol	Parameter	Min	Typ	Max	Unit	Notes / Condition
Input Requirement						
Vin	Main input voltage		1.80		V	Supplied by V1P8A
Cin	V1P2S_IN		100		nF	
Output Requirement						
Vnom	Nominal output voltage		1.2		V	
Vtol	Output voltage tolerance	-2%		+2%		
Cout	Output capacity		2.2		µF	
Iout-DC	Output load current		1	50	mA	
IQSC	Quiescent current (operational)		10		µA	Iout-DC = 0mA
IQSC	Quiescent current (sleep)		2		µA	Iout-DC = 0mA
PSRR	Power supply rejection ratio	50			dB	Noise = 0.1Vpp, 1-10kHz, ½ Iout-DC
Vnoise	Output Noise	50		100	µVRMS	10-100kHz, ½ Iout-DC

Table 25: V1P2S Truth Table

V1P2S_CTRL.			
V1P2S_SEL	V1P2S_EN	SLP_S3_B	V1P2S
1	0	1	Off
1	1	1	On
x	x	0	Off

V1P2SX:

This voltage rail is used to supply the SoC SFR via an internal switch from VDDQ.

Table 26: V1P2SX Power Switch Specification

Description	Value [max, mΩ]
Input power path board resistance	20
Output power path board resistance	20
Input, output rails wirebond & internal FET RDS-ON	160

The maximum current is 155mA, switched internally and controlled via the SoC SLP_S0iX_B signal.

9.6.7 Power Rail VSYSU

VSYSU is the voltage rail that sources power of VSYS through an external power switch. This power domain is used to source communication and the modem. The external power switch is generated via a P-channel FET.

MYXPM6021 provides an enable signal VSYSU_EN_B supplied by VSYS, driving the gate of the external FET. The MYXPM6021 also provides a feedback input signal VSYSU_FB to control the slew rate and limit the inrush current.

VSYSU external P-channel power switch parameters:

Rdson (Vgs=4V)	15-35mohm
Input capacitance, Ciss	750-2315pF
Output capacitance, Coss	265-900pF
Reverse transfer capacitance, Crss	240-800pF

9.6.8 Power Rail VSYS_SX

VSYSU is the voltage rail that sources power of VSYS through an external power switch. The external power switch is generated via a P-channel FET.

MYXPM6021 provides an enable signal VSYSSX_EN_B, supplied by VSYS, driving the gate of the external FET. The MYXPM6021 also provides a feedback input signal VSYSSX_FB to control the slew rate and limit the inrush current.

VSYS_SX external P-channel powe switch parameters:

Rdson (Vgs=4V)	15-35mohm
Input capacitance, Ciss	750-2315pF
Output capacitance, Coss	265-900pF
Reverse transfer capacitance, Crss	240-800pF

9.6.9 Power Rail VSYS_S

VSYS_S is a voltage rail that is supplied by VSYS through an internal MYXPM6021 power switch with a RDSon of 900mΩ.

Table 27: VSYS_S Power Switch Specification

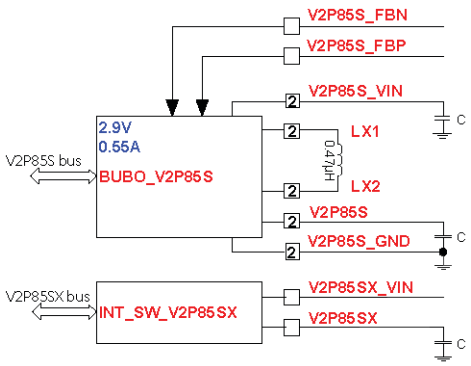
Description	Value [max, mΩ]
Input, output rails wirebond & internal FET RDS-ON	1,000

VSYS_S power switch is enabled when SLP_S3_B is high, unless VSYS_S_CTRL.VSYS_S_SEL bit is set to high.

9.6.10 Buck Boost Regulator V2P85S

The MYXPM6021 integrates a buck/boost converter supplying 2.85V into the system for touch screen, eMMC, sensors and V2P85SX loads. The maximum output current of V2P85S buck/boost regulator is 550mA.

Figure 20: Buck Boost V2P85S Power Domain Block Diagram



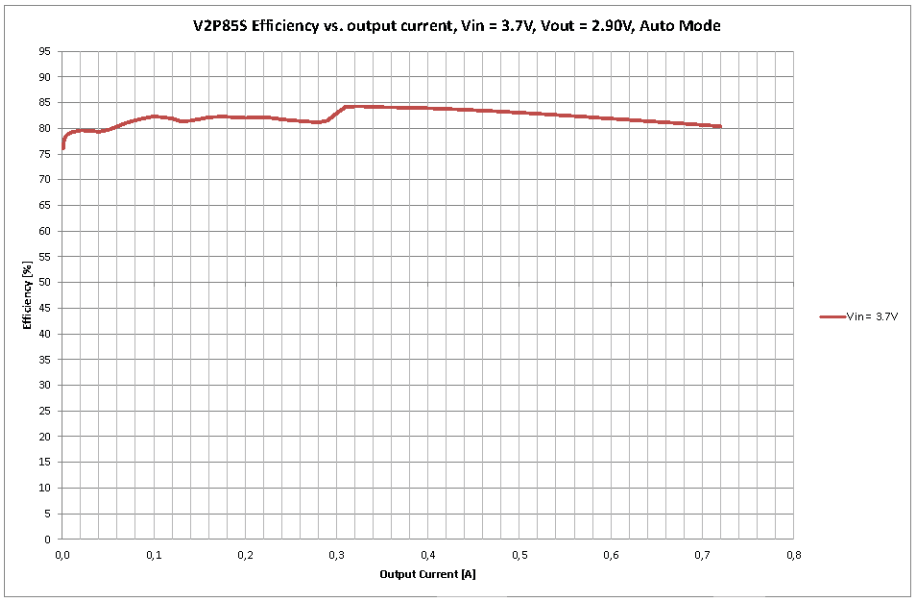
9.6.10.1 Electrical Characteristics V2P85S

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V2P85S_VIN	Input voltage		2.7		4.5	V
Cin	At V2P85S_IN			4.7		µF
Cout				2 x 22		µF
ESR of output capacitor				6 @ 22µF		mΩ
ESL of output capacitor				1.6 @ 3MHz		nH
L_BUCK	Inductor value		-20%	0.47	+20%	µH
L_DCR	Inductor resistance				48	mΩ
V2P85S	Output Voltage	IOUT= Imax		1.24/1.35±2%		V
F_BUCK/BOOST	Frequency of operation			3		MHz
Transient load current profile		0-550mA		250		ns
Transient droop[1]		0-550mA			116	mV
Transient overshoot[2]		550-0mA			116	mV
Ton	Turn on time				2	ms
Rpd	Discharge impedance	V2P85S .. 0V			20	Ω
IQ_OFF	Quiescent current in off mode				50	µA
Normal Mode – Synchronous rectification (PWM)						
Maximum Output Current (Imax)			550			mA
ILIMIT Current limitation		Cycle by cycle	850			mA
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 21		
Sleep Mode – Pulse skipping (PSK)						
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 21		

Notes:

1. Including DC accuracy, ripple and load regulation
2. Including DC accuracy, ripple and load regulation
3. RDSON meansurement on ATE

Figure 21: V2P85S Efficiency



9.6.10.2 V2P85S Subsystems

V2P85SX:

The main purpose of this voltage rail is to provide power for cameras. The control of this power rail is derived from the SoC SLP_S0ix_B signal. The maximum current is 250mA. The internal switch has a R_{DSon} of 460mΩ.

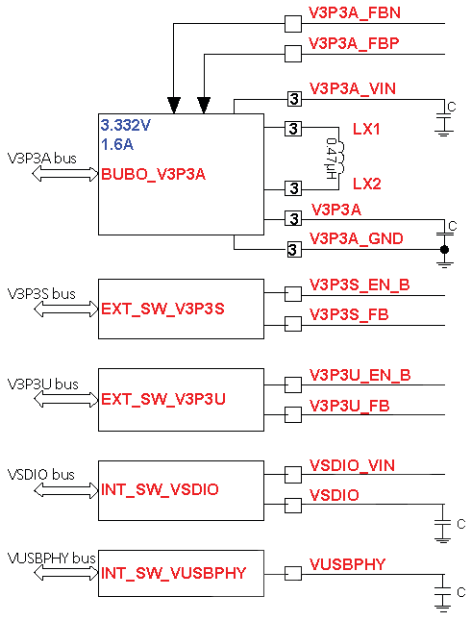
Table 28: V2P85SX Power Switch Specification

Description	Value [max, mΩ]
Input power path board resistance	0
Output power path board resistance	40
Input, output rails wirebond & internal FET RDS-ON	180

9.6.11 Buck Boost Regulator V3P3A

The MYXPM6021 integrates a buck/boost converter supplying 3.3V into the system towards the SoC, V3P3U, V3P3S, VUSBPHY and VSDIO. The output voltage is set to 3.33V. The maximum output current of V3P3A buck regulator is 1600mA.

Figure 22: V3P3A Power Domain Block Diagram



9.6.11.1 Electrical Characteristics V3P3A

Table 29: Electrical Parameter for BUCKBOOST_V3P3A

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V3P3A_VIN Input Voltage	Input voltage		2.7		4.5	V
Cin	at V3P3A_IN			4.7		µF
Cout				2 x 47		µF
ESR of output capacitor				6 @ 22µF		mΩ
ESL of output capacitor				1.6 @ 3MHz		nH
L_BUCK	Inductor value		-20%	0.47 or 2x1	+20%	µH
L_DCR	Inductor resistance				48	mΩ
V3P3A	Output voltage	IOUT= Imax		3.33±2%		V
F_BUCK/BOOST	Frequency of operation			3		MHz
Transient load current profile		150-1519mA		250		ns
Transient droop[1]		150-1519mA			13	mV
Transient overshoot[2]		1519-150mA			133	mV
Ton Turn on time					2	ms

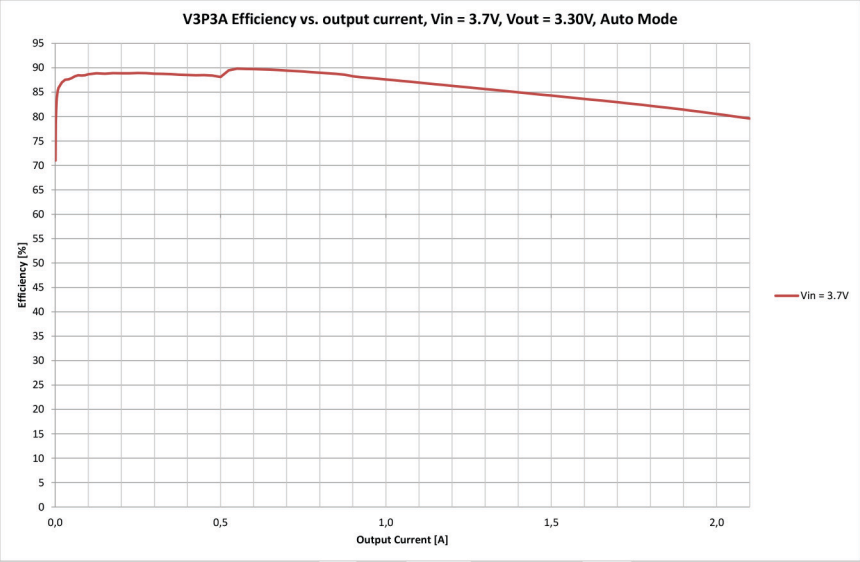
Table 29: Electrical Parameter for BUCKBOOST_V3P3A (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
IQ_ON	Quiescent current in on mode				50	µA
Rpd	Discharge impedance	V2P85S .. 0V			20	Ω
Normal Mode – Synchronous Rectification (PWM)						
Maximum Output Current (Imax)			1570			mA
ILIMIT	Current limitation	Cycle by cycle	1.3*Imax			mA
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 23		
Sleep Mode – Pulse Skipping (PSK)						
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 23		

Notes:

1. Including DC accuracy, ripple and load regulation
2. Including DC accuracy, ripple and load regulation

Figure 23: V3P3A Efficiency



9.6.11.2 V3P3A Subsystems

V3P3U:

V3P3U is the voltage rail which is sourced by V3P3A and switched by an external P-channel FET. This voltage rail is primarily for Wi-Fi and Bluetooth support. The MYXPM6021 provides a control signal V3P3_U_EN supplied by V3P3A and derived from SoC's SLP_S4_B signal. The maximum current for this power rail is 700mA.

V3P3U external P-channel power switch parameters:

Rdson (Vgs=4V)	35-62.5mohm
Input capacitance, Ciss	750-2000pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	100-360pF

V3P3S:

V3P3S is the voltage rail which is sourced by V3P3A and switched by an external P-channel FET. The voltage domain is used to power the display, MIPI LVDS bridge, SSD drive and audio codecs. The control signal V3P3S_EN_B is supplied by V3P3A and when asserted low, the signal slew rate is controlled to limit the in-rush current when the external P-channel FET turns on.

V3P3S external P-channel power switch parameters:

Rdson (Vgs=4V)	35-62.5mohm
Input capacitance, Ciss	750-2000pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	100-360pF

VUSBPHY:

VUSBPHY is composed of V3P3A or VSYS via an internal power rail switch. It sources power from V3P3A whenever the V3P3A buck boost converter is enabled. When V3P3A is switched off VUSBPHY is sourced by VSYS.

Table 30: VUSBPHY Power Switch Specification

Description	Value [max, mΩ]
V3P3A input power path board resistance	10
VSYS input power path board resistance	10
Output power path board resistance	20
Input, output rails wirebond & internal FET RDS-ON	305

VSDIO:

This voltage rail supplies power to the SDIO/MMC subsystem. The voltage rail is either supplied by 1.8V via V1P8_A buck converter or by V3P3_A. In case of a 3.3V supply, the internal switch has a R_{DSon} of 200mΩ, in case of 1.8V the R_{DSon} is 80mΩ. The maximum current is 200mA.

Table 31: VSDIO Power Switch Specification

Description	Value [max, mΩ]
V3P3A input power path board resistance	10
VSYS input power path board resistance	10
Output power path board resistance	20
Input, output rails wirebond & internal FET RDS-ON	108

The table below shows how the VSDIO voltage is selected:

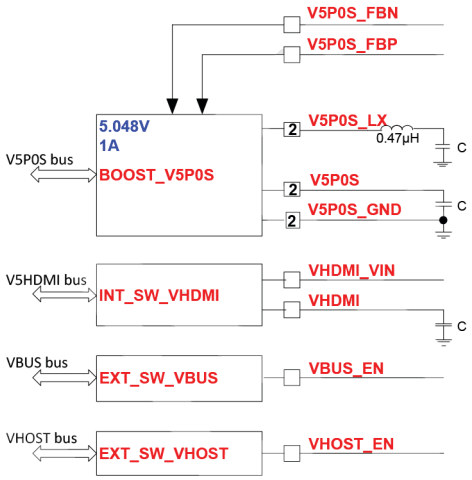
Table 32: VSDIO Output Voltage Selection

DMMC3_PWR_EN_B	SDMMC2_1P8_EN	VSDIO
0	0	0
0	1	0
1	0	3.3V
1	1	1.8V

9.6.12 Boost Regulator V5P0S

The MYXPM6021 integrates a boost converter to supply 5V for HDMI, USB3, VBUS & USB2/3 OTG. The maximum output current of V5P0_S boost converter is 955mA.

Figure 24: V5P0S Power Domain Block Diagram



9.6.12.1 Electrical Characteristics V5P0S

Table 33: Electrical Parameter for BOOST_V5P0S

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V5P0S_VIN	Input Voltage		2.7		4.5	V
Cin	At V5P0S_IN			2 x 22		µF
Cout				2 x 10		µF
ESR of output capacitor				6 @ 22µF		mΩ
ESL of output capacitor				1.6 @ 3MHz		nH
L_BOOST	Inductor value		-20%	0.47	+20%	µH
L_DCR x	Inductor value				48	mΩ
V5P0S	Output Voltage	IOUT= Imax		5.0±2%		V
F_BOOST	Frequency of operation			3		MHz
Transient load current profile		0-955mA		250		ns
Transient droop[1]		0-955mA			202	mV
Transient overshoot[2]		1519-150mA			202	mV
Ton	Turn on time				2	ms
IQ_OFF	Quiescent current in off mode				50	µA
Normal Mode – Synchronous Rectification (PWM)						
Maximum Output Current (Imax)			1570			mA

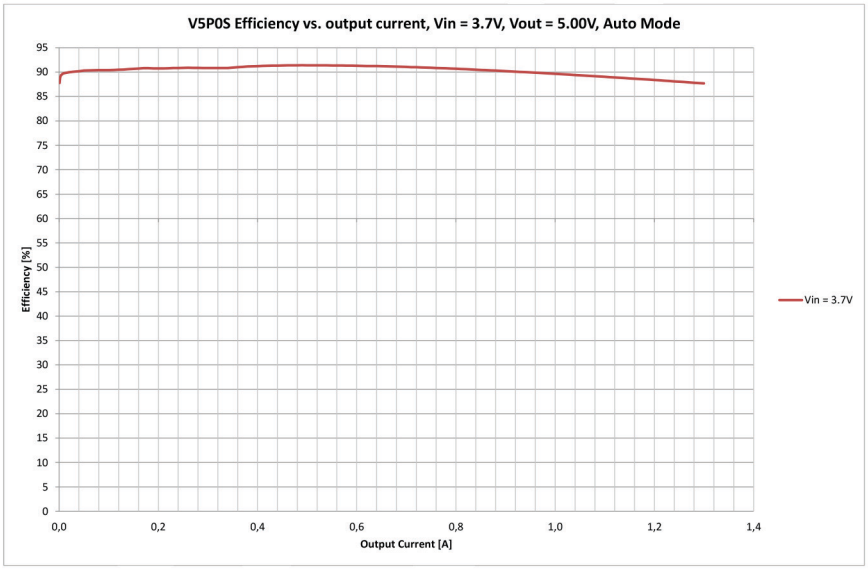
Table 33: Electrical Parameter for BOOST_V5P0S (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
ILIMIT	Current limitation	Cycle by cycle	1.3*Imax			mA
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 25		
Sleep Mode – Pulse Skipping (PSK)						
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 25		

Notes:

1. Including DC accuracy, ripple and load regulation
2. Including DC accuracy, ripple and load regulation

Figure 25: V5P0S Efficiency



9.6.12.2 V5P0S Subsystems

VHOST:

This voltage rail is used for the 5V VBUS providing power to the USB2/3 host, switched by an external power switch.

The maximum current of this power domain is 900mA.

Table 34: VHOST external power switch driver capability

Parameter	Value
V_IL	>0.66V
V_IH	<1.1V
I_EN	>0.5µA

VBUS:

VBUS is the power rail supplying the VBUS of USB2/3 OTG through an external power switch.

The maximum current of this power domain is 900mA.

Table 35: VBUS external switch driver capability

Parameter	Value
V_IL	>0.66V
V_IH	<1.1V
I_EN	>0.5µA

VHDMI:

VHDMI is the 5V power supply to the HDMI connector sourced by V5P0S through an internal switch. The RDSon of the internal switch is 900mΩ.

Table 36: VHDMI Power Switch Specification

Description	Value [max, mΩ]
Input power path board resistance	20
Output power path board resistance	200
Input, output rails wirebond & internal FET RDS-ON	1200

The maximum current of this power domain is 55mA.

9.6.13 VLP Low Power Regulator

The LDO_LP will be used for running the internal sequencer. It is supplied by the system supply voltage VSYS. This allows a power up prior to the system power domains. This LDO acts as the supply for the bias, reference, OTP and MYXPM6021 registers.

Electrical Characteristics (Ta = -40 to +85 ºC) VSUP = 2.7 to 4.5V.

Table 37: Electrical Parameter for LDO_LP

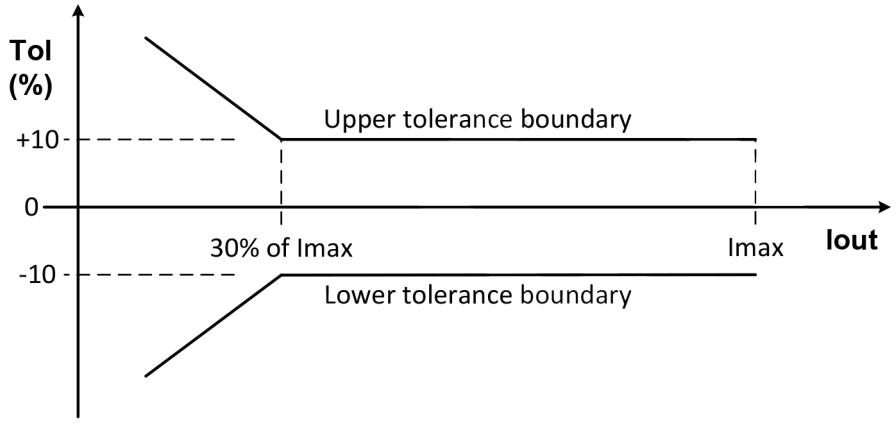
Parameter	Description	Test Conditions	Min	Typ	Max	Unit
VSYS1 / VSYS2	Input Voltage		2.7		4.5	V
VLP	Output Voltage	IOUT= Imax	2.45	2.5	2.55	V
Accuracy		Room temperature			0.6	%
Cstab	Stabilization Capacitor	Tolerance of ± 35%	2.2			µF
Cdec	Decoupling Capacitor	Tolerance of ±35%	220	1.6 @ 3MHz		nF
Cesr	ESR of Capacitor	F > 1MHz		0.1		Ω
IMAX Current	Maximum Output		10			mA
IQ_ON	Quiescent Current in ON MODE				10	µA
PSRR	Power Supply Rejection Ratio	Noise = 0.1VPP, 1-10kHz, ½ Iout	50		60	dB
Vnoise	Output Noise	BW = 10-100kHz, ½ Iout	60		100	µV
Ton	Turn on time from POR		5	10		ms

9.7 Current Monitor

The following switching regulators include an output current measurement feature: VCC, VNN, V1P0A, V1P05S and VDDQ. The output current is measured internally and averaged across 1ms. The average current is digitalized by using the 10 bit ADC (refer to ADC section) and stored into 2 x 8 bits registers for each mentioned voltage rail as specified. The average current is updated to the respective registers once every 1ms.

The current measurement tolerance target for each of the voltage rails mentioned above is as below:

Figure 26: Current Measurement Tolerance Boundary



Form #: CSI-D-685 Document 011

Table 38: Current Measurement Resolution

Voltage Rail	Resolution	Tolerance
VCC	20mA/LSB	±5%
VNN	20mA/LSB	±5%
V1P0A	5mA/LSB	±5%
V1P05S	2.5mA/LSB	±5%
VDDQ	5mA/LSB	±5%

10 I2C Interface

10.1 Overview

The MYXPM6021 is a slave-only device that is mastered by the SoC. It resides off the SoC's I2C. The slave device implemented on MYXPM6021 side is an asynchronous implementation and will support the high speed mode (3.4MHz). Some of the main features for the I2C slave are:

- MYXPM6021 is accessed using a 7-bit addressing scheme.
- The interface draws minimum power when not actively reading/writing registers.
- The slave adapts to the incoming frequency without any communication as the protocol for fast mode and high speed mode is the same.
- 2 Slave Address are supported. Each address is targeting a 256 register page inside MYXPM6021.
- Sequential offset accesses within a single transaction (burst reads and writes) are not required.

10.2 Slave Addresses

The MYXPM6021 supports the standard I2C read and write functions. The configuration register space is divided into two 256-byte partitions. The MYXPM6021 supports five 7-bit device addresses to access each of the 256 byte partitions. Note that in 8-bit format, these addresses correspond to 0xBC and 0xDC for writes, and 0xBD and 0xDD for reads.

In order to avoid conflict with the assigned addresses the slave addresses will be programmable via OTP.

Table 39: I2C Slave Addresses

	Slave Address	Read Address	Write Address
Device 1	0x5E	0xBC	0xBD
Device 2	0x6E	0xDC	0xDD

The slave addresses need to be locked in order to avoid that software can overwrite them and disable the communication.

10.3 Protocol

Reads from PMIC registers follow the "combined protocol" as described in the I2C specification, in which the first byte written is the register offset to be read, and the first byte read (after a repeat START condition) is the data from that register offset. See the figures below for details. The following diagrams capture the different highspeed and fast-speed transaction format/protocol

Figure 27: I2C Fast Speed Write

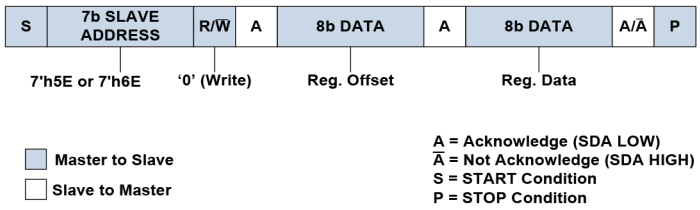


Figure 28: I2C Fast Speed Read

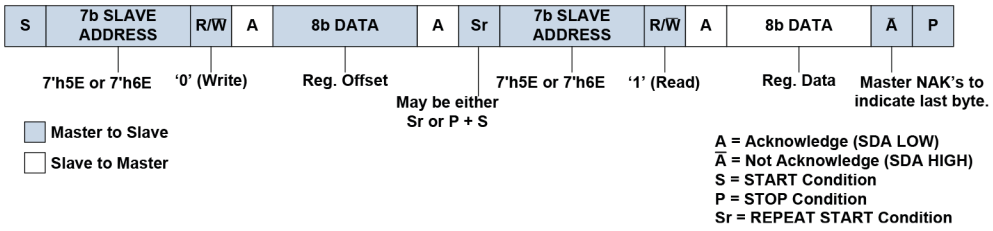


Figure 29: High Speed Write

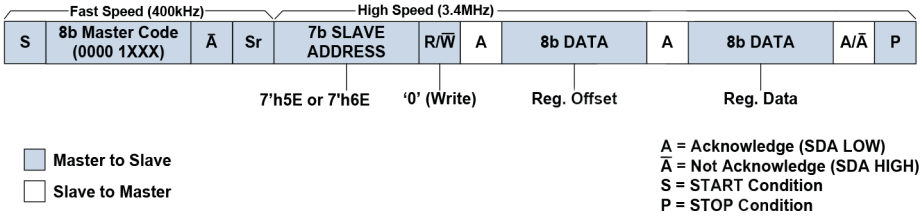
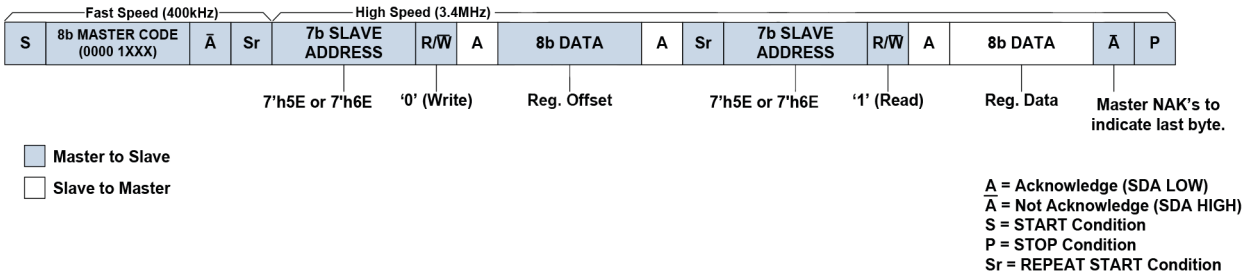


Figure 30: High Speed Read



10.4 Electrical Requirements

Table 40: I2C Signal Electrical Specification

Parameter	Min	Nom	Max	Units	Notes
Voltage (VDD)	1.71	1.8	1.89	V	At pin
Vil			0.3*VDD	V	
Vih	0.7*VDD			V	
Vhys	0.1			V	
Vol			0.2*VDD	V	
Cpin	2		5	pF	
Tfall_hs	10		40	ns	3.33 Mb/s Operation
Tfall_fs	20		300	ns	400 Kb/s Operation
Tr/Tf	30		70	%	Measurement Points

11 External EEPROM Controller

11.1 Overview

During the initial power-on sequence the content of the OTP is copied into the sequencer execution registers. Since the OTP registers can only be programmed during the manufacturing & testing process, the EEPROM controller function provides the possibility of overwriting the sequencer execution registers in the field and/or as backup.

During initial power-on the EEPROM access will always be interrogated. EEPROM reading and register copying depend on a valid signature inside the EEPROM. Therefore the EEPROM has to be supplied from a dedicated external power rail or directly from the main battery. If a valid signature is not read, MYXPM6021 operates with the register setting based on the OTP registers.

11.2 Electrical Characteristics

Table 41: EEPROM Signal Electrical Specifications

Parameter	Min	Nom	Max	Units	Notes
Voltage	1.71	1.8	1.89	V	At pin
Vil			0.3*VDD1	V	
Vih	0.7*VDD1			V	
Vhys	0.1			V	
Vol			0.2*VDD1	V	
Cpin	2		5	pF	
fmax			125	kHz	
Trise_fs	20		300	ns	Pull-up resistor is integrated in MYXPM6021
Tfall_fs	20		300	ns	Full Speed Operation
Tr/Tf	30		70	%	Measurement Points

11.3 Functions

- The internal CLKGEN provides a 125kHz clock signal to the EEPROM I2C master clock output.
- An EEPROM read is internally initiated by MYXPM6021 power sequence state machine.
- EEPROM initial address EEPROM_SIGN_ADDR, defined by Register Bit written by OTP is read first to see if EEPROM is connected and data at initial address is correct. If one of these two conditions is not fulfilled, EEPROM data will not be copied into any registers.

- In the case where the EEPROM is connected and data at initial address SIGN_ADDR is correct, EEPROM content from SIGN_ADDR + 1 to end address STOP_ADDR will be copied to the registers starting at address register SIGN_ADDR = SIGN_ADDR + 1.
- There is a status register in MYXPM6021 implemented to indicate the status of EEPROM connection, the signature matching and data copying.

12 Power Source Detection

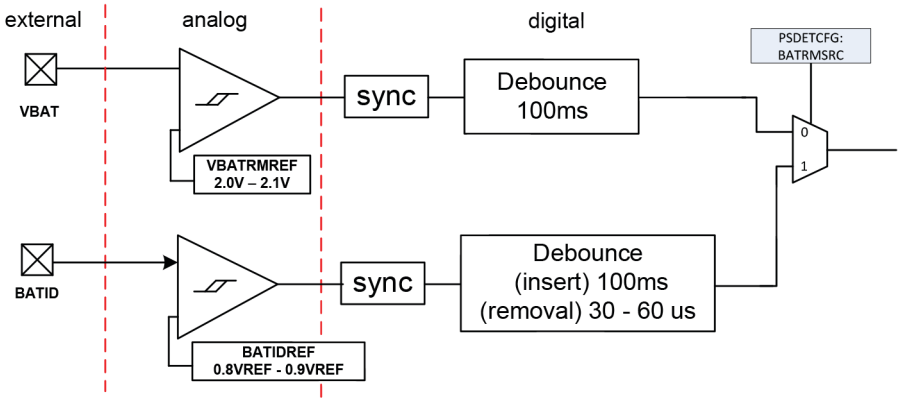
12.1 Overview

There are three input supply sources that can be detected by MYXPM6021: VBAT, VDCIN_SENSE and VBUS_SENSE referring to the battery, AC adapter and USB connector, respectfully. For all power sources dedicated comparators are used for the power detection. All detectors include de-bounce logic with a nominal time period of 100ms which can be disabled by software.

12.2 VBAT Power Source Detection

12.2.1 Battery Voltage Monitor & Removal / Insertion Detection

Figure 31: VBAT Input Detection



It is advantageous to use a battery pack with integrated BSI resistance (pull-down in the battery pack indicating the ID or size) as it offers an advanced warning on battery removal events. Such an implementation is necessary to meet the SDWN_B signal timing requirement of some modem SIM cards.

During normal operation (battery pack present/inserted), the BSI resistance in the battery pack pulls the analog voltage at the BATID pin to an intermediate voltage, between VREF (ADC bias voltage from the VREFB pin) and GND. When the BSI terminal of the battery pack no longer makes contact (as on removal), BATID is immediately pulled high to VREF by the measurement resistance on the platform, RMBI (30KΩ to 200KΩ).

While using the BATID comparator sensing the battery insertion / removal, there are separate de-bounce times for insertion and removal. This provides sufficient power-up time for USB PHY related components on insertion, on the other hand it allows a quick detection time of battery removal for SIM card early warning (via SDWN_B).

Note that BAITD comparator is giving a low output if the battery is removed.

When BATRMSRC=1 (using BATID comparator), the thresholds in the table below define the present/absent voltage trip

points. Note that when using the BATID comparator to sense battery insertion / removal, there are separate debounce times for insertion and removal. This is to allow for sufficient power-up sequencing of USB PHY related components on insertion, and also allow for quick detection of battery removal for SIM card early warning (via SDWN_B).

Table 42: BATID Comparator Threshold

Parameter	Description	Min	Typ	Max	Unit
V'BATIDREFH	BATID Rising threshold (L->H, indicating battery removal)	Typ-0.025	0.9*Vref	Typ+0.025	V
V'BATIDREFL	BATID Falling threshold (H->L, indicating battery insertion)	Typ-0.025	0.8*Vref	Typ+0.025	V
tDEBOUNCE insert	BATID Presence Comparator Debouncing Time (Insertion)	90	100	110	ms
tDEBOUNCE remove	BATID Presence Comparator Debouncing Time (Removal)	30		62	µs

The second method detecting a battery removal is while monitoring the battery voltage itself via a battery voltage comparator. The table below specifies the thresholds of the battery removal comparator.

Table 43: VBAT removal Comparator Threshold

Parameter	Description	Min	Typ	Max	Unit
V'BATRMREFH	VBAT Rising Threshold (L->H, indicating battery insertion)	2.075	2.1	2.125	V
V'BATRMREFL	VBAT Falling Threshold (H->L, indicating battery removal)	1.975	2.0	2.025	V
tDEBOUNCE	Battey Voltage Comparator Debouncing Time (Insertion and removal)	90	100	110	ms

12.2.2 Battery Pack Interface

The BATID pin can be used to support three possible functions: digital battery communication, analog measurement of an ID resistance, and/or analog battery presence detection.

This digital communication is intended to be left generic, with simple pass through level shifters to/from the host on 2 discrete pins. The intent is to be protocol agnostic to provide support for many standards. The figure below illustrates the multiple uses of BATID.

Figure 32: Battery Single Wire Block Diagram for Analog Sensing, Digital Communication

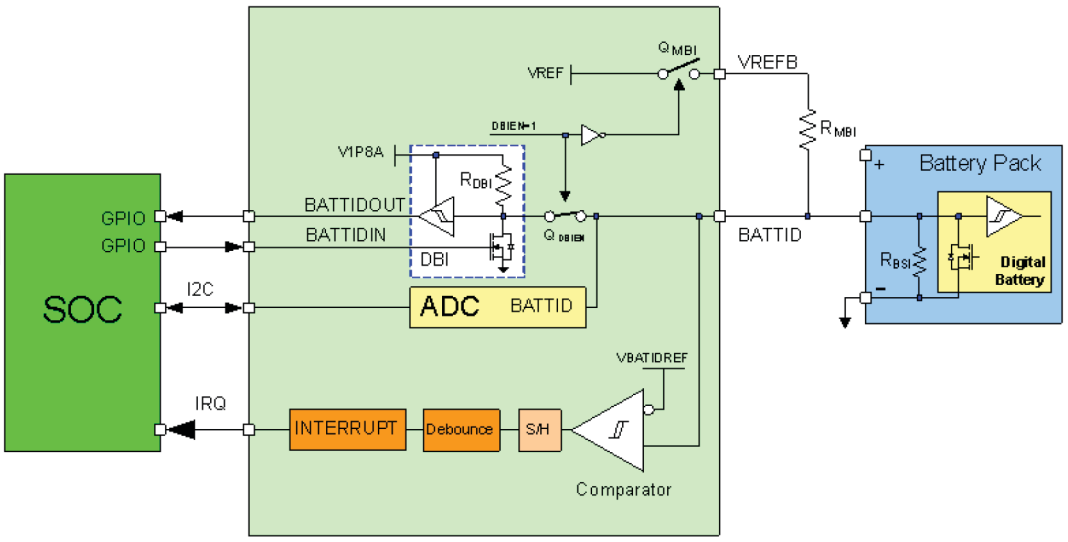


Table 44: BATID Electrical Specification

Parameter	Min	Nom	Max	Units	Notes
Frequency	3.268		250	kHz	Digital communication
Voltage	1.71	1.8	1.89	V	
Vil			0.35	V	
Vih	0.9			V	
Vhys	0.05			V	
Vol			0.01	V	1mA source current
Cload			380	pF	
Trise			500	ns	0V to Vih(min)
Tfall			500	ns	Vpu to Vil(max)

12.2.3 Battery Presence Detection

Normally the BSI resistor will pull the voltage on the BATID line to a level that is lower than a set trip point. If the battery is removed, the BATID node will be pulled high by the R_{MBI} platform resistor which is typically in the range of 30KΩ to 200KΩ. When this occurs, MYXPM6021 detects that the battery is being removed (if configured).

The integrated 100ms de-bounce logic ensures there are no false removal alerts. Depending on the MYXPM6021 setting either a complete Cold Off sequence will be performed or an interrupt to the SOC will be sent.

If the DBIEN bit be set, allowing digital battery communication mode to be entered on the BATID pin, the battery presence logic is switched off to avoid battery removal detection. Prior to Digital Battery Communication, MYXPM6021 retains the

last known BATID line voltage value in order to ensure that no false battery removal events are reported.

12.2.4 BSI Sensing

MYXPM6021 is able to detect the presence of the R_{BSI} resistor as shown. The R_{BSI} is a 1% resistor and can range anywhere from 0 to 130kΩ. MYXPM6021 is able to differentiate between different ID resistances (assuming standard 1% values over the aforementioned range).

12.2.5 Digital Battery Communications

MYXPM6021 includes level shifting hardware that will take the single BATID line and convert it to two unidirectional 1.8V I/O signals, BATIDIN and BATIDOUT. The SOC will communicate with the battery digital interface via MYXPM6021 which is transparent and shifts the signals from the battery voltage domain to the 1.8V SOC domain. GPIO0P1 and GPIO0P2 pins are used for this function.

Software, based on the value of the BSI resistance discovered, may choose to enable digital battery communication.

Whenever digital communication is enabled (DBIEN bit in the BATDETCTRL register), MYXPM6021 disables the analog BATID presence sensing logic, and will not falsely report removal events.

Table 45: Digital Battery Interface Specification

Parameter	Min	Nom	Max	Units	Notes
Voltage (VDD)	1.71	1.8	1.89	V	At pin
Vil			0.3*VDD	V	
Vih	0.7*VDD			V	
Vhys	0.1			V	
Vol			0.2*VDD	V	
Voh	VDD-0.45			V	
Trise	20		300	ns	
Tfall	20		300	ns	
Tr/Tf	30		70	%	Measurement points

12.2.6 System Voltage Monitor

The System Voltage Monitor is used to indicate when the voltage level on the VSYS pin has settled above 3.0V. This is implemented using a simple comparator and fixed thresholds. The voltage level on VSYS must stay above 3.0v for a minimum of 100ms (i.e. debounce time) before the output will become active.

Figure 33: VSYS Valid Input Power Detection

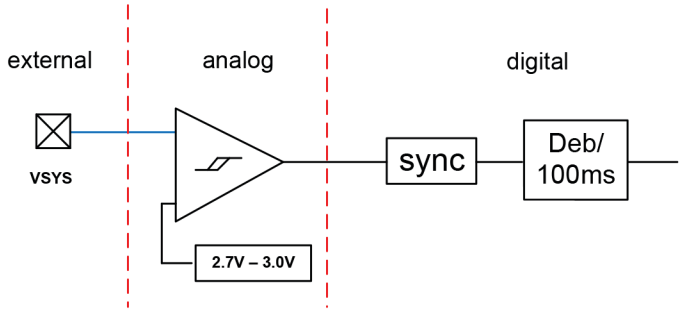


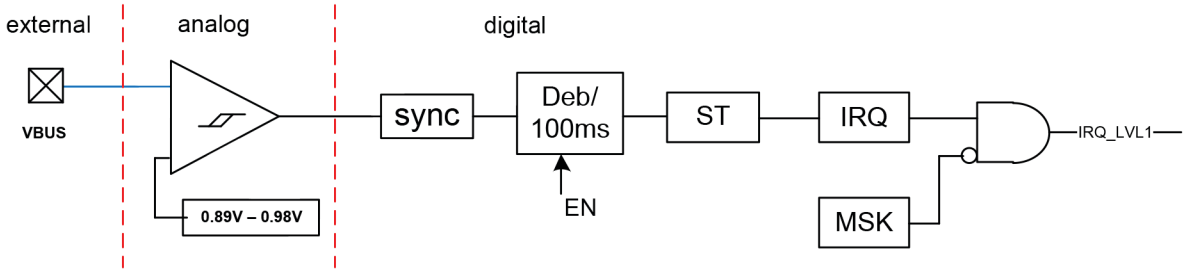
Table 46: VSYSREF Definition

Parameter	Description	Min	Typ	Max	Unit
VSYSREFH	VSYS Rising Threshold (VSYS: L->H)	2.975	3.0	3.035	V
VSYSREFL	VSYS Falling Threshold (VSYS: H->L)	2.675	2.70	2.725	V
tDEBOUNCE	VSYS comparator debouncing time	90	100	110	ms

12.3 VBUS Power Source Detection

The VBUS Power Source Detector is used to indicate when the voltage level on the VBUS pin has settled above ~ 940mV.

Figure 34: USB Detection



VBUS Rising (Connection Event)

When the VBUS level at the comparator becomes higher than the reference voltage (including rising edge hysteresis), VBUS is considered valid. If the VBUSDBEN bit is set in the VBUSDETCTRL register, VBUS must be sensed as valid for the full 100ms de-bounce time before the SVBUSDET bit in the SPWRSRCIRQ register is set, indicating charger connection. If VBUSDBEN is cleared, SVBUSDET is set immediately upon VBUS becoming valid.

VBUS Falling (Disconnection Event)

When the VBUS level at the comparator becomes lower than reference voltage (including falling edge hysteresis), VBUS is considered invalid. If the VBUSDBEN bit is set in the VBUSDETCTRL register, VBUS must be sensed as invalid for

the full 100ms de-bounce time before the SVBUSDET bit in the SPWRSRCIRQ register is cleared, indicating charger disconnection. If VBUSDBEN is cleared, SVBUSDET is cleared immediately upon VBUS becoming invalid.

On any change in the SVBUSDET bit in the SPWRSRCIRQ register (set or clear), the corresponding interrupt flag, VBUSDET, is set in the PWRSRCIRQ 2nd-level interrupt register. This automatically sets the PWRSRC interrupt flag in the IRQLVL1 interrupt register, and alerts the SOC. The SOC is expected to query the SVBUSDET bit in SPWRSRCIRQ to determine if the event was a connection or disconnection.

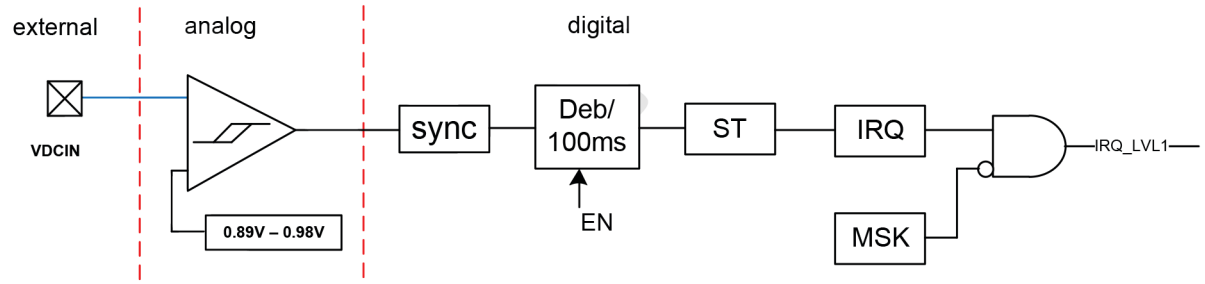
Table 47: VBUS Detection, Analog Electrical Parameters

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Rising Threshold			895	940	990	mV
Falling Threshold			810	860	900	mV
Hysteresis			65	80	90	mV
Dynamic Parameters						
Rising Delay			1	10	20	us
Falling Delay			1	10	20	us

12.4 VDCIN Power Source Detection Comparators

The VDCIN Power Source Detector is used to indicate when the voltage level on the VDCIN pin has settled above ~ 940mV.

Figure 35: VDCIN Detection



The same sequence of operation as with VBUS is followed for boot-up. An interrupt is generated based upon the detection of power applied or removed from the VDCIN pin.

VDCIN Rising (Connection Event)

When the VDCIN level at the comparator becomes higher than the reference voltage (including rising edge hysteresis), VDCIN is considered valid. If the VDCINDBEN bit is set in the VDCINDETCTRL register, VDCIN must be sensed as valid for the full 100ms de-bounce time before the SDCINDET bit in the SPWRSRCIRQ register is set, indicating adapter connection. If VDCINDBEN is cleared, SDCINDET is set immediately upon VDCIN becoming valid.

VDCIN Falling (Disconnection Event)

When the VDCIN level at the comparator becomes lower than the reference voltage (including falling edge hysteresis), VDCIN is considered invalid. If the VDCINDBEN bit is set in the VDCINDETCTRL register, VDCIN must be sensed as invalid for the full 100ms de-bounce time before the SDCINDET bit in the SPWRSRCIRQ register is cleared, indicating charger disconnection. If VDCINDBEN is cleared, SDCINDET is cleared immediately upon VDCIN becoming invalid.

On any change in the SDCINDET bit in the SPWRSRCIRQ register (set or clear), the corresponding interrupt flag, DCINDET, is set in the PWRSRCIRQ 2nd-level interrupt register. This automatically sets the PWRSRC interrupt flag in the IRQLVL1 interrupt register, and alerts the SOC. The SOC is expected to query the SDCINDET bit in SPWRSRCIRQ to determine if the event was a connection or disconnection.

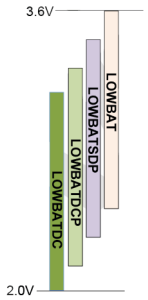
Table 48: VDCIN Detection, Analog Electrical Parameters

Parameter	Symbol	Min	Typ	Max	Unit
VDCIN Rising Threshold (VDCIN: L->H)	VDCINREFH	895	940	990	mV
VDCIN Falling Threshold (VDCIN H->L)	VDCINREFL	810	860	900	mV
Debouncing		90	100	110	ms

12.5 BATLOW Definition

Once detection is done, according to the supply configuration, the ADC will be triggered to measure the VBAT voltage. The result register will be compared with one of the four possible threshold levels defined to generate the BATLOW signal. This is needed in order to decide if the system can boot or not. The below figure shows the levels and the explanation for the different LOWBAT levels.

Figure 36: Valid Battery Thresholds



- LOWBAT: No supply source detected apart from the main battery.
- LOWBATSDP: VBUS_SENSE detected and USB is of the SDP type.
- LOWBATDCP: VBUS_SENSE detected and USB is of the DCP, CDP or ACA type.
- LOWBATDC: VDCIN_SENSE is detected so an AC adapter is connected.

After every battery measurement the result will be compared with the corresponding thresholds. If the system is running on AC/DC plug or USB supply the VBAT input voltage is measured frequently with the ADC. If the level drops below

an appropriate threshold the PMIC will assert the BATLOW pin, the processor will then take action. All thresholds are preprogrammed in OTP and can be overwritten by software.

12.6 Power Source Detection Events

The events generated from the Power Source Detection Logic and driven into the event interface are:

- Battery Insertion Event.
- Battery Removal Event.
- USB Insertion Event.
- USB Removal Event.
- DCIN Insertion Event.
- DCIN Removal Event.
- VSYS Valid Event

All power source detection events will generate an Interrupt towards the SoC.

- Battery wake-up
- AC/DC wake-up
- USB wake-up

12.7 Wake-Up Logic

In order to make a decision about when the system can wakeup, SYSCO evaluates the status for each power supply source and the power button. The following table shows the wakeup events, conditions, and results.

Table 49: System Wake-Up Condition

Events	Condition to be Fulfilled	Comments
Battery Insertion	BATWAKEEN = 1 BATLOW_B = 1	Regardless of other power supply's status.
AC Adapter Insertion	ADPWAKEEN = 1 BATLOW_B = 1 DCBOOT = 0	Dependency on battery status
	ADPWAKEEN = 1 BATLOW_B = 1 DCBOOT = 1	No dependency on battery status
USB Insertion	USBWAKEEN = 1 BATLOW_B = 1 Battery Present	Wakeup is not allowed if running only on USB.

Table 49: System Wake-Up Condition (continued)

Events	Condition to be Fulfilled	Comments
Battery Becomes Valid	BATLOW_B = 1 ADPWAKEEN = 1	Battery present. AC/DC insertion event (DCBOOT = 0). The wakeup is only delayed till battery is charged enough (VBAT > BATLOW).
	BATLOW_B = 1 USBWAKEEN = 1	Battery present. USB insertion event. The wakeup is only delayed till battery is charged enough.
Power Button	BATLOW_B = 1	System running on battery
	PWRBTNWAKE.USBWAKE = 01 PWRBTNWAKE.USBWAKE = 10	Battery present and charging from USB. Battery still not charged enough. 01 = Wakeup due to DCP charging source. 11 = Wakeup due to SDP (500mA) source. If the battery can only source 100mA, then the system will not boot.
	PWRBTNWAKE.ACDCWAKE = 1 DCBOOT = 0	Battery present and charging from AC/DC. Battery still not charged enough.
	DCBOOT = 1 BSTRMDETRN = 0	Wakeup immediately

12.8 MYXPM6021 Catastrophic and Critical Events

There are 9 “catastrophic and critical events” which may force an immediate Cold Off, i.e. force an immediate hardware-controlled VR shutdown, or simply alert the SOC. Four of these events – BCU VCRIT, BATRM, System TEMP and battery TEMP – may have configurable action, programmed via the I2C register map. These events are split into two categories: “Catastrophic” and “Critical” Catastrophic events are:

- THERMTRIP_B - The SOC asserts THERMTRIP_B in response to an SOC over-temperature condition. MYXPM6021 asserts SDWN_B immediately. After 90us, shuts down all VRs.
- PMICTEMP – MYXPM6021 detects a critical over-temperature condition on its internal die sensor and asserts SDWN_B immediately. After 90us, shuts down all VRs.
- System TEMP – MYXPM6021 detects a critical over-temperature condition on an external system thermistor. If programmed MYXPM6021 asserts SDWN_B immediately. After 90us, shuts down all VRs.
- Battery TEMP – MYXPM6021 detects a critical over-temperature condition on an external battery thermistor. If programmed MYXPM6021 asserts SDWN_B immediately. After 90us, shuts down all VRs.
- VSYSUVP – MYXPM6021 detects VSYS “undervoltage” (VSYS ≤ 2.7V) by VSYS under voltage hard-coded comparator for more than 100µs.MYXPM6021 asserts SDWN_B immediately. After 90us, shuts down all VRs.
- VSYSOVP – MYXPM6021 detects VSYS “overvoltage” (VSYS ≥ 5.4V min) by VSYS over voltage hard-coded comparator for more than 100µs.MYXPM6021 asserts SDWN_B together with shutting down all VRs immediately.

- VBATRM – MYXPM6021 detects that a battery was removed from the system by VBAT comparator when the bit BATRMSRC in the PSDETCTRL register is cleared (=0).

Critical events are:

- IDBATRM – MYXPM6021 detects that a battery was removed from the system by BATID presence comparator when the bit BATRMSRC in the PSDETCTRL register is set (=1). All VRs are shut down in sequenced order but without waiting for SLP_S*_B from SOC.
- BCU VCRIT – The BCU detects that the VSYS voltage node has entered the “VCRIT” operating zone.

13 Analog–to–Digital Converter

A general purpose analog-to-digital converter (GPADC) provides measurements of various voltages, currents and temperatures within the device. There is one 10-bit ADC which is time-division multiplexed to perform the measurements of the various parameters. The GPADC contains the 10-bit ADC, the analog input channel multiplexer and some additional analog functions.

13.1 Electrical Characteristics

Table 50: ADC Electrical Charakteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC Resolution				10		bit
Absolute Accuracy			12		15	mV
Integral Non-Linearity	INL			+/- 2		LSB
Differential Non-Linearity	DNL			+/- 0.8		LSB
ADC Supply Voltage				2.5		V
ADC Reference Voltage	VADC_REF	VDD_CORE		2.5		V
ADC Operating Current		During conversion		100		µA
Power Down Current					1	µA
ADC Clock				1		MHz
Auto-Zero Time				3		us
Total Sampling Time		Including the Auto-Zero time		10		us
Conversion Time				11		us
Total ADC Conversion Time				21		us
Maximum Source Impedance	R_S	RS is the impedance of the external source sampled by the ADC			120	kΩ
Internal Mux Resistance	R_{INT}			5		kΩ
Internal Sampling Capacitor	C_S			10		pF
Total Input Capacitance	C_{INT}	Parasitic and pad capacitance included		11		pF
Acquisition Time		~7τ = 7 x (RS + RINT) x CINT			10	us
VSYS Voltage Range / Channel A0 /		ADC=[(VSYS-2.5) x 0.5] x 1023 gain = 0.8	2.5		5.5	V

Table 50: ADC Electrical Charakteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC_IN1÷3 Voltage Range / channels A1, A2, A3 /		ADC=[VIN / 2.5] x 1023 gain = 1.0	0		2.5	V
Internal Temp. Sensor Voltage / channel A4 /		ADC=[1 – 1.2 x VTJ] x 1023 gain = 3.0	0		0.833	V
VBBAT Voltage Range / channel A5 /		ADC=[1 - 0.2 x VBBAT] x 1023 gain = 0.5	0		5	V
Inter Channel Isolation		80dB for channel A3 (ADC_IN6)		60		dB
Regulator OV/UV monitoring Channel A8 ÷ A10		Gain =0.5	0		5.5	V

13.2 Analog Overview

The AD conversion is of successive approximation type using sample and hold. It has a resolution of 10 bits and a conversion cycle of 21 clock cycles including an auto-zero phase (23 cycles consumed back-to-back). The GPADC is supplied from the same supply, VDDCORE, as the digital block. If unused, the GPADC can be disabled to reduce its power consumption by a factor around 100.

The GPADC has an analog input multiplexer with 16 input channels.

Table 51: ADC Channel Overview

CH	Description	Signal Name	Measurement Range	Condition	Comment	ADC Value	Gain
0	Battery Voltage, VBAT (Pin:IBATSENSE)	VREG	0.0V.. 5.0V	Yes		0.5* Vin/VLP*1 023	0.5
1	Battery ID (Pin: BATID)	ADCIN1	0.0V .. VLP	No	VREFB needs to be switched on 1ms prior to ADC measurement. VREFB needs to stay on when battery removal has to be detected by the VBATID Comparator.	Vin/VREF B*1023	1
2	MYXPM6021 Die Temperature (no pin)	vbe_ADC/ adc_temp	0.0V .. VLP/3	Yes		3* Vin/VLP *1023	3
3	Battery Pack Temp 0 (Pin: BPTHERM0)	ADCIN2	0.0V .. VLP	No	VREFT needs to be switched on 1ms prior to ADC measurement.	Vin/VREF T *1023	1
4	Battery Pack Temp 1 (Pin: BPTHERM1)	ADCIN3	0.0V .. VLP	No		Vin/VREF T*1023	1
5	System Temp 0 (Pin: SYSTHERM0)	ADCIN4	0.0V .. VLP	No		Vin/VREF T*1023	1

Table 51: ADC Channel Overview (continued)

CH	Description	Signal Name	Measurement Range	Condition	Comment	ADC Value	Gain
6	System Temp 1 (Pin: SYSTHERM1)	ADCIN5	0.0V .. VLP	No	VREFT needs to be switched on 1ms prior to ADC measurement.	Vin/VREF T*1023	1
7	System Temp 2 (Pin: SYSTHERM2)	ADCIN6	0.0V .. VLP	No		Vin/VREF T*1023	1
8	VSYS (Pin: VSYS)	VSYS	2.5V .. 5.5V	Yes		0.8*(VSYS - VLP)/VLP* 1023	0.8
9	Averaging Output Current	ADCIN7	0.0V .. VLP	Yes	There is a pre-selection on which rail the current measurement will be averaged	2*Vin/VRE F*1023	2

14 System Voltage & Temperature Monitoring

14.1 Overview

The system voltage and temperature monitoring allows high power, high temperature events as well as the system voltage monitoring. These functions allow several system conditions to be monitored by MYXPM6021, taking autonomous action and informing the SoC on system voltage and temperature events.

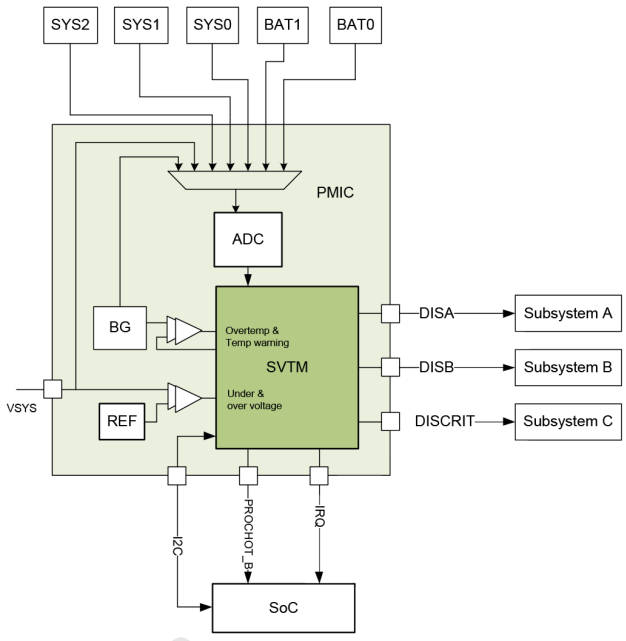
The SVTM will monitor the following:

- System Voltage Input VSYS: in SOC_S0 via the ADC channel 8
- MYXPM6021 onDie Temperature: this is done via a comparator in real time and via ADC channel 2
- Battery Temperature: 2 ADC channels (channel 3 & 4)
- Platform Temperature: 3 ADC channels (channel 5, 6 & 7)
- Under Voltage: A comparator flags this event
- Over Voltage: A comparator flags this event

In reaction to either threshold crosses or a flag coming from several comparators the SVTM will drive several pins on MYXPM6021 for use by the processor and to other platform components. Depending on the condition it can generate warnings, and/or interrupts and can generate a shutdown event.

14.2 Block Diagram

Figure 37: SVTM Block Diagram



14.3 Backup Battery Management

Configuration and status registers of MYXPM6021, and timekeeping logic (powered by a platform voltage rail VRTC) in the SOC are backed-up by a super capacitor or coin cell battery in case of SOC power loss (e.g., main battery changed). The VRTC is supplied usually through a diode by either V3P3A or VBATBKUP with V3P3A taking priority whenever it is available. If a SOC power loss is of an extended duration, the back-up supply will fall below the minimum operational voltage, VMIN, and the content of the registers will be lost and reset to default value.

14.3.1 Backup Battery Charger

The Backup Battery Charger is used to charge coin cell Li-Ion batteries or “Super-capacitors”. Due to the chemistry and/or relatively high internal resistance of these batteries it is necessary to charge in two stages: a constant current stage; and a constant voltage stage. In essence this means that the charger acts as a currentlimited voltage source. The target voltage and maximum charge current are configurable via separate 2-bit register settings.

In addition to battery charging the circuit must protect against discharging of the backup battery in cases when the system supply drops below the backup battery voltage. For this reason an always-on protection circuit is utilized which shuts off the reverse current path as required.

To facilitate low power system modes wherein no oscillator is running, the Backup Battery Charger is capable of autonomously self-regulating its state such as to stop charging when the battery is full and to start once again when the battery is sufficiently emptied.

14.3.2 Power Consumption

The MYXPM6021 logic supplied by the VRTC domain will consume <5µA.

15 General Purpose IOs

15.1 Overview

The MYXPM6021 provides 16 GPIO pins under the control of the SoC. The majority of these GPIO pins have a default configuration as CMOS inputs with weak (50 KOhm) pull downs enabled. The GPIO buffers support operation as open-drain or push pull outputs. They are split into 2 groups, each with a different fixed supply:

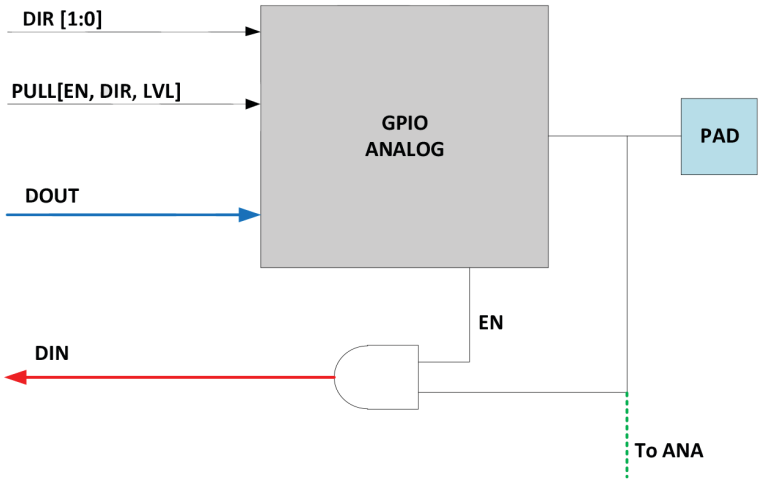
- GPIO0P0 – GPIO0P7 support a level of 1.8V
- GPIO1P0 – GPIO1P7 support 3.3V

Following are the supported feature from the digital GPIO IP:

- CMOS or Open Drain output and input configuration
- 2k-ohm or 50k-ohm pull-up or pull-down resistance
- Read back of output PAD values
- Output Level select by register
- Digital glitch filter of 62µs
- Digital filter (de-bouncer, typically 32ms) with programmable bypass
- Interrupt and interrupt mask functionality.
- Polarity selection (default active high)
- Analog/Digital Input
- Alternate input/output functionality.

15.2 Analog Block, Control & Data Signals

Figure 38: GPIO Block Diagram



As shown in Figure 38 above, there are 5 signals which control the analog behavior of the GPIO pin. Note that EN is generated from the analog pad block itself.

The following tables show the coding for configuring the GPIO pads.

Table 52: GPIO Direction Configuration

DIR		GPIO Configuration
0	0	Input Analog
0	1	Input Digital
1	0	Output Open-Drain
1	1	Output CMOS

Table 53: GPIO Pull-Up/Pull-Down Configuration

PULL_EN	PULL_DIR	PULL_LVL	GPIO Configuration
0	X	X	No pull-up / pull-down
1	0	0	2-KOhm pull-down
	0	1	50-KOhm pull-down
	1	0	2-KOhm pull-up
	1	1	50-KOhm pull-up

16 External Battery Charger Control

16.1 Overview

The PMIC has the ability to control an external battery charger IC. In order to determine the appropriate input current limit for the charger during certain scenarios, the CHGDET_B pin is asserted or de-asserted by the USB PHY on the platform depending on output current capability of the USB charger detected.

ILIM0 and ILIM1 pins of MYXPM6021 will output signals to the charger to set the charger input current limit. The external charger is capable of generating an interrupt which will be forwarded to the SoC via MYXPM6021. This interrupt will come from the CHGRINT_B pin. During charging the battery temperature will be monitored.

16.2 Charger Current Limit

The external charger input current limits are set according to the table below.

Table 54: External Charger Current Limits

CHRDET_B	ILIM1	ILIM0	Power Source	Input Current Limit
1	0	0	USB DCP	More than 100mA, usually 1.5A
1	0	1	USB SDP	100mA
1	1	1	USB SDP	500mA
X	1	0	AC/DC Adapter	Customer specific, limited by max charger output current

The AC/DC adapter usually takes priority over the USB charger as input power to the external battery charger. However, MYXPM6021 detects the AC/DC adapter by monitoring VDCIN_SENSE. MYXPM6021 changes ILIM0 and ILIM1 level immediately VDCIN_SENSE fall below the internal voltage reference threshold to inform the external charger to lower its current limit at the removal of AC/DC adapter.

Table 55: Charger Control Pins

Name	Dir	Voltage	Signal Description
CHGRINT_B	I	VSYS	Battery charging status and fault interrupt from charger IC, active low. Internal 10kOhm pull-up to VSYS. 0=interrupt, asserted with a minimum pulse width of 200µs
ILIM[1:0]	O	VSYS	External charger input current limits
CHGDET_B	I	VUSBPHY	USB DCP detection. Asserted by USBPHY when it detected a charger that can source more than 100mA Internal 100kOhm pull-up to VSYS 1=SDP detected 0=DCP or CDP/ACA

17 Interrupt Controller

17.1 Overview

The interrupt control unit maintains the state of the First Level IRQ tree and is responsible for asserting and deasserting the MYXPM6021's IRQ to the application SoC. It contains status bits for interrupts from all the second-level sub-blocks. If unmasked, the second-level interrupts will propagate to the appropriate first-level interrupt bit, as assigned below. If the first-level interrupt is unmasked, it will propagate to the IRQ pin, which will remain high as long as unmasked interrupts have not been cleared.

17.2 First Level Interrupt

The MYXPM6021 interrupt signal IRQ signal is connected to a GPIO of the SoC indicating MYXPM6021 unmasked events to be investigated by the SOC while reading the IRQ status registers via I2C.

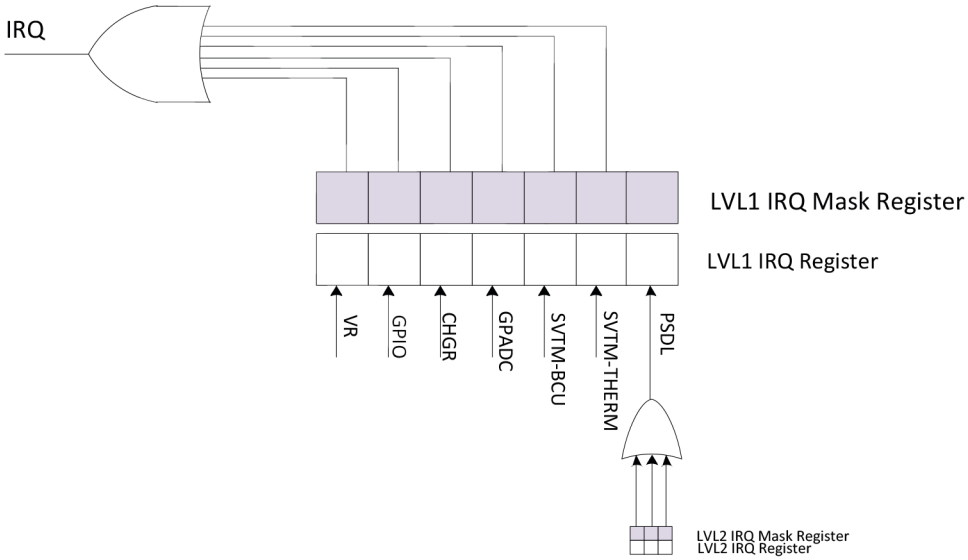
The MYXPM6021 interrupt scheme contains two levels. The first-level interrupt register contains 6 IRQ bits, and indicates which PMIC sub-block triggered the interrupt. One bit is dedicated to each of the interrupt-causing MYXPM6021 sub-blocks. For all units, the second-level interrupt registers indicate the specific interrupt triggers for each sub-block. A masking system is provided to enable or disable specific interrupt handlers.

If any bits are set in the first-level IRQ mask, the assertion of an interrupt from the masked sub-block(s) will not cause an assertion of the IRQ signal, nor will it set the first-level IRQ bit. By limiting the first-level IRQ bits set to only those that are unmasked; this disambiguates the dispatching of interrupts.

First-Level IRQ bits may not be directly cleared; they are cleared by clearing all unmasked second-level IRQ bits, and then are implicitly cleared.

When all unmasked first-level IRQ bits are implicitly cleared (all unmasked second-level interrupts directly cleared), the IRQ pin is de-asserted.

Figure 39: 1st Level Interrupt



17.3 Second Level Interrupt

While First-Level Interrupt bits inform the interrupt handler of which sub-block interrupted, second-level interrupt registers/ bits provide the interrupt handler with the specific nature of the block‘s interrupt event.

If any bits are set in a second-level interrupt mask, then the appropriate second level interrupt bit is prevented from asserting the first level interrupt bit for the corresponding sub-block, nor will the bit become set. (Only unmasked 2nd level interrupt bits may be set).

The table below summarizes the second level interrupts.

Table 56: Second Level Interrupt

Interrupt Name	Register	Source	First-Level Interrupt	Related Status Bit	Description
VBUSDET	PWRSRCIRQ	Input Power Source Detection	PWRSRC	SVBUSDET	Indicates that a valid VBUS voltage is detected or removed.
DCINDET	PWRSRCIRQ	Input Power Source Detection	PWRSRC	SDCINDET	Triggered when a AC/DC adapter has been detected or removed.
BATDET	PWRSRCIRQ	Input Power Source Detection	PWRSRC	SBATDET	Interrupt is triggered when a battery is connected or disconnected.
SYS0ALRT0	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 0 temperature thermal alert0 occurs

Table 56: Second Level Interrupt (continued)

Interrupt Name	Register	Source	First-Level Interrupt	Related Status Bit	Description
SYS1ALRT0	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 1 temperature alert0 occurs
SYS2ALRT0	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 2 temperature alert0 occurs
PMICALRT0	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a PMIC die temperature alert0 occurs
SYS0ALRT1	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 0 temperature alert1 occurs
SYS1ALRT1	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 1 temperature alert1 occurs
SYS2ALRT1	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 2 temperature alert1 occurs
PMICALRT1	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a PMIC die temperature alert1 occurs
SYS0CRIT	THRMIRQ1	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 0 critical temperature event occurs
SYS1CRIT	THRMIRQ1	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 1 critical temperature event occurs
SYS2CRIT	THRMIRQ1	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 2 critical temperature event occurs
PMICCRIT	THRMIRQ1	Thermal Control Unit	THRM		Set by the thermal state machine when a PMIC die critical temperature event occurs
BAT0ALRT0	THRMIRQ2	Thermal Control Unit	THRM		Set by the thermal state machine when a battery thermistor 0 temperature alert0 occurs
BAT1ALRT0	THRMIRQ2	Thermal Control Unit	THRM		Set by the thermal state machine when a battery thermistor 1 temperature alert0 occurs
BAT0ALRT1	THRMIRQ2	Thermal Control Unit	THRM		Set by the thermal state machine when a battery thermistor 0 temperature alert1 occurs

Table 56: Second Level Interrupt (continued)

Interrupt Name	Register	Source	First-Level Interrupt	Related Status Bit	Description
BAT1ALRT1	THRMIRQ2	Thermal Control Unit	THRM		Set by the thermal state machine when a battery thermistor 1 temperature alert1 occurs
BAT0CRIT	THRMIRQ2	Thermal Control Unit	THRM		Set by thermal state machine when a battery thermistor 0 critical temperature event occurs
BAT1CRIT	THRMIRQ2	Thermal Control Unit	THRM		Set by thermal state machine when a battery thermistor 1 critical temperature event occurs.
VWARNBIRQ	BCUIRQ	BCU	BCU		Triggers whenever the VSYS voltage crosses the VWARNB threshold, rising or falling.
VWARNAIRQ	BCUIRQ	BCU	BCU		Triggers whenever the VSYS voltage crosses the VWARNA threshold, rising or falling.
VCRITIRQ	BCUIRQ	BCU	BCU		Triggers whenever the VSYS voltage crosses the VCRIT threshold, rising or falling.
VBAT	ADCIRQ0	ADC	ADC		Bit is set after completion of VBAT manual conversion if not masked
BATID	ADCIRQ0	ADC	ADC		Bit is set after completion of BATID manual conversion if not masked
PMICTEMP	ADCIRQ0	ADC	ADC		Bit is set after completion of PMIC die temperature manual conversion if not masked
BPTHERM0	ADCIRQ0	ADC	ADC		Bit is set after completion of BPTHERM0 manual conversion if not masked
BPTHERM1	ADCIRQ0	ADC	ADC		Bit is set after completion of BPTHERM0 manual conversion if not masked
SYSTHERM0	ADCIRQ0	ADC	ADC		Bit is set after completion of SYSTHERM0 manual conversion if not masked
SYSTHERM1	ADCIRQ0	ADC	ADC		Bit is set after completion of SYSTHERM1 manual conversion if not masked
SYSTHERM2	ADCIRQ0	ADC	ADC		Bit is set after completion of SYSTHERM2 manual conversion if not masked

Table 56: Second Level Interrupt (continued)

Interrupt Name	Register	Source	First-Level Interrupt	Related Status Bit	Description
CHRG	CHGRIRQ	Charger Control Unit	CHGR		Triggered when an interrupt input from the external discrete charger is generated.
GPIOxPx	GPIOIRQ	GPIO	GPIO	DINxPx	Each GPIO pin can be configured as input with programmable interrupt edge for rise, fall or both.
VHDMIOCP	VHDMIIRQ	VHDMI	VHDMIOCP		Bit is set when VHDMI over current condition occurs if not masked

18 Power Button & Utility Button

18.1 Overview

The system has two buttons that can be used together to trigger the system to power “on” or “off” in different ways.

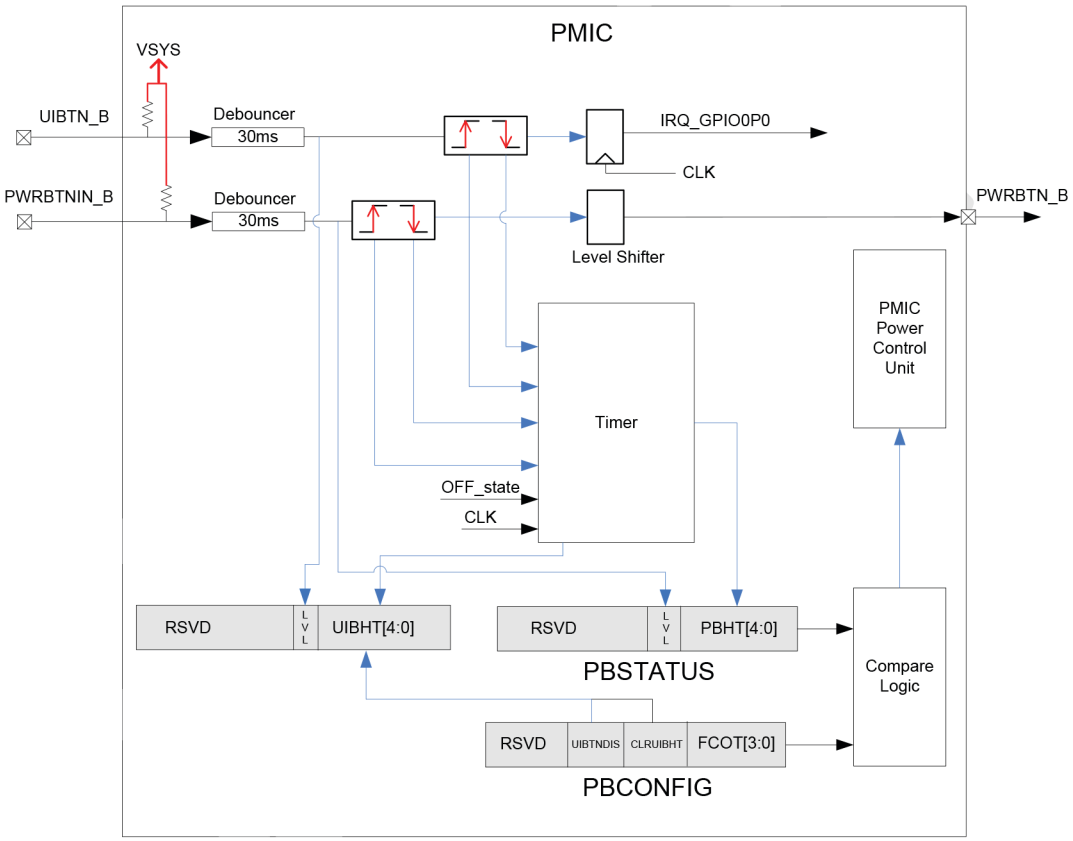
The main power button (PWRBTNIN_B) is an active-low input with an internal pull-up resistor to VSYS.

The second button is the Utility button or user interface button (UI button, UIBTN_B). This button is typically used as a home button and also includes the pull-up resistor to VSYS.

Both buttons are de-bounced with a 30ms filter and supervised by a timer unit measuring the pulse length.

18.2 Power/Utility Button Block Diagram

Figure 40: Power/Utility Button Detection Logic



18.3 PWRBTNIN_B Electrical Parameters

Table 57: PWRBTNIN_B Pad Thresholds

	L->H Vth, high	H->L Vth, low	Vhyst
	[mV]	[mV]	[mV]
Min	672.5	577.5	95
Typ	927.5	732.5	195
Max	1158.5	860.5	298

19 Pulse Width Modulation Generation

19.1 Overview

The PWM block is used to generate up to three PWM signals on three dedicated output pins. Mainly they are used to drive display backlight circuits. All the PWM outputs can be enabled on demand.

19.2 Functional Description

Each of the PWM outputs are able to generate output frequencies from ~23.44 KHz down to ~183Hz in 128 steps.

- f= (6MHz/256) / (FREQ+1)

The duty cycle can be selected between 1/256 to 256/256 (always high).

19.3 PWM output signals

There are 3 PWM output signals (PWM[2:0]) on MYXPM6021.

Table 58: PWM Output Signals

Name	I/O	Voltage Level	Pin Mode	Pin Level	Internal pu/pd
PWM[2:0]	O	1.8V	CMOS	Low	No

20 Panel Control

20.1 Overview

The MYXPM6021 provides two pins for display panel control, BACKLIGHT_EN to enable the display backlight circuit and PANEL_EN to enable the display panel electronics. The buffers driving these pins are slew-rate controlled push-pull output buffers similar to the GPIOs, each capable of high-voltage (3.3V) operation.

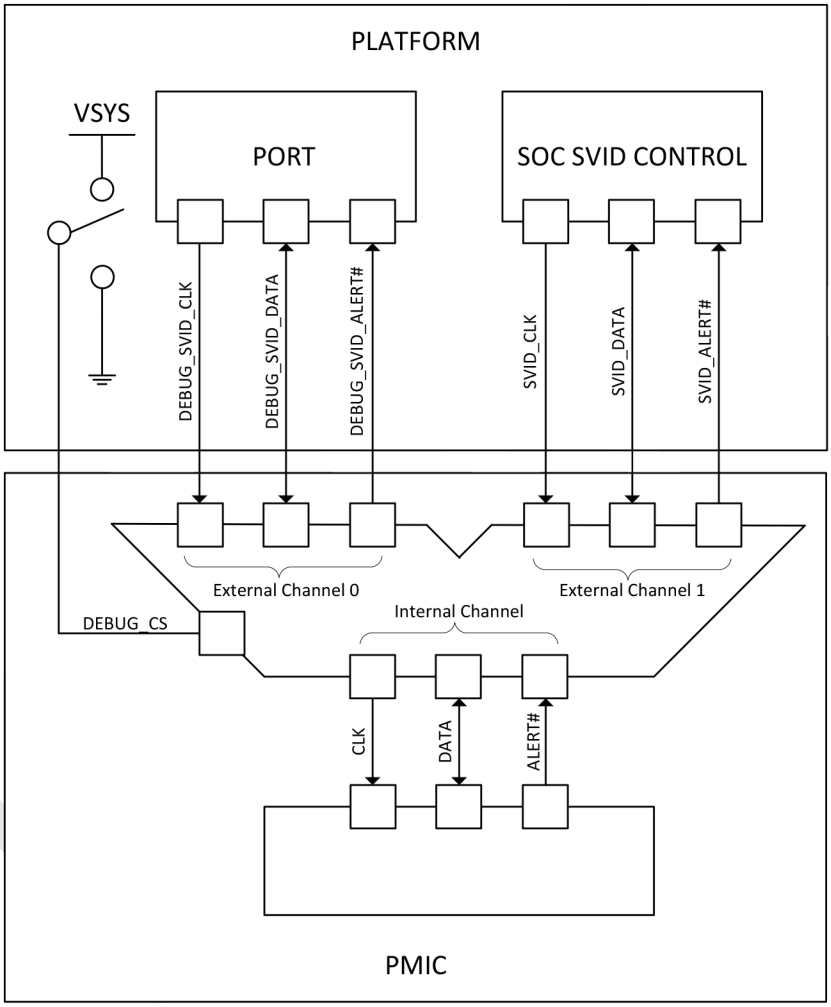
21 Debug Ports

There are 2 debug ports, one for the SVID and another one for the I2C interface.

21.1 SVID Debug Port

When in SVID debug mode, the PMIC SVID buffers connected to the SOC/CPU will be disabled and communication is redirected to an external bus master using a secondary set of pins. This will enable external control of the PMIC interface without any SOC/CPU bus contention. In addition, the debug channel enables a point to point bus topology with the external bus master, thereby providing clean signal integrity. The DEBUG_CS signal is used to disable SOC SVID transmission during debug. This will ensure that the SOC does not hang waiting for PMIC SVID responses.

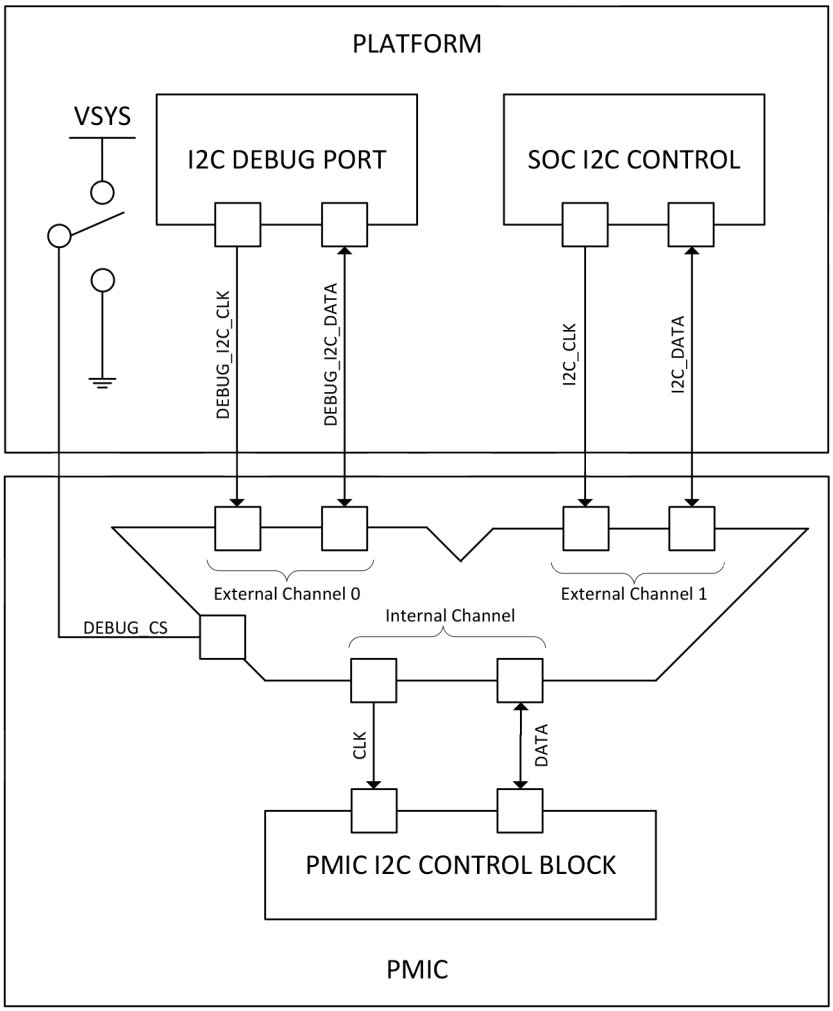
Figure 41: SVID Debug Port Bus Diagram



21.2 I2C Debug port

When in I2C debug mode, the MYXPM6021 I2C buffers connected to the SOC will be disabled and communication is redirected to an external bus master using a secondary set of pins. This will enable external control of the MYXPM6021 interface without any SOC/CPU bus contention. In addition, the debug channel enables a point to point bus topology with the external bus master, thereby providing clean signal integrity.

Figure 42: I2C Debug Port Bus Diagram



22 Package Information

22.1 MYXPM6021 Package Details

22.1.1 Pin Description, Pin Out

Below is the pin description list of MYXPM6021. In the type column the following abbreviations are used:

- PS, VSS Power Supply
- DI, DO, DIO Digital Input, Digital Output, Digital Input/Output
- AI, AO, AIO Analog Input, Analog Output, Analog Input/Output
- OD Open-Drain Output

22.1.2 Ball Order

Table 59: MYXPM6021 Ball Order

Ball	Name	Type	Description
A1	VSYS41	PS	System power supply
A2	VSYS43	PS	System power supply
A3	VNN_IN2A	PS	VNN buck regulator supply voltage
A4	VNN_IN2B	PS	VNN buck regulator supply voltage
A5	VNN_IN3A	PS	VNN buck regulator supply voltage
A6	VNN_IN3B	PS	VNN buck regulator supply voltage
A7	VNN_IN4A	PS	VNN buck regulator supply voltage
A8	VNN_IN4B	PS	VNN buck regulator supply voltage
A9	VSYS_4	PS	System power supply
A10	V1P8A_INA	PS	V1P8A buck regulator supply voltage
A11	V1P8A_INB	PS	V1P8A buck regulator supply voltage
A12	VDDQ_IN1A	PS	VDDQ buck regulator supply voltage
A13	VDDQ_IN1B	PS	VDDQ buck regulator supply voltage
A14	VDDQ_IN2A	PS	VDDQ buck regulator supply voltage
A15	VDDQ_IN2B	PS	VDDQ buck regulator supply voltage
A16	V2P85S_INA	PS	V2P85S buck boost supply voltage
A17	V2P85S_INB	PS	V2P85S buck boost supply voltage

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
A18	V2P85S_A	AO	V2P85S output voltage
A19	V2P85S_B	AO	V2P85S output voltage
A20	VCCAPWROK	DO	VCCAPWROK output signal
A21	V1P2SX_IN	AI	V1P2SX input supply
A22	V2P85SX_IN	PS	V2P85SX input supply
A23	V1P2S	AO	V1P2S output voltage
A24	VSYS33	PS	System power supply
A25	VSYS32	PS	System power supply
B1	VSYS42	PS	System power supply
B2	VNN_LX2A	AO	VNN buck LX node phase 2
B3	VNN_LX2B	AO	VNN buck LX node phase 2
B4	VNN_LX3A	AO	VNN buck LX node phase 3
B5	VNN_LX3B	AO	VNN buck LX node phase 3
B7	VNN_LX4B	AO	VNN buck LX node phase 4
B8	DGND1	VSS	Ground
B9	V1P8S_IN	AI	V1P8S input supply
B10	V1P8A_LXA	AO	V1P8A buck LX node
B11	V1P8A_LXB	AO	V1P8A buck LX node
B12	VDDQ_LX1A	AO	VDDQ buck LX node phase 1
B13	VDDQ_LX1B	AO	VDDQ buck LX node phase 1
B14	VDDQ_LX2A	AO	VDDQ buck LX node phase 2
B15	VDDQ_LX2B	AO	VDDQ buck LX node phase 2
B16	V2P85S_LX1A	AO	Buck boost V2P85S LX node 1
B17	V2P85S_LX1B	AO	Buck boost V2P85S LX node 1
B18	V2P85S_LX2A	AO	Buck boost V2P85S LX node 2
B19	V2P85S_LX2B	AO	Buck boost V2P85S LX node 2
B20	DGND11	VSS	Ground
B21	V1P2SX	AO	V1P2SX output voltage
B22	V2P85SX	AO	V2P85SX output voltage
B23	DGND12	VSS	Ground

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
B24	DGND13	VSS	Ground
B25	VSYS31	PS	System power supply
C1	VNN_IN1B	PS	VNN buck regulator supply voltage
C2	VNN_LX1B	AO	VNN buck LX node phase 1
C3	VNN_GND1A	VSS	Ground
C4	VNN_GND2A	VSS	Ground
C5	VNN_GND3A	VSS	Ground
C6	VNN_GND4A	VSS	Ground
C7	DGND3	VSS	Ground
C8	DGND4	VSS	Ground
C9	V1P8S	AO	V1P8S output voltage
C10	V1P8A_GNDA	VSS	Ground
C11	V1P8A_GNDB	VSS	Ground
C12	VDDQ_GND1A	VSS	Ground
C13	VDDQ_GND1B	VSS	Ground
C14	VDDQ_GND2A	VSS	Ground
C15	VDDQ_GND2B	VSS	Ground
C16	V2P85S_GNDA	VSS	Ground
C17	V2P85S_GNDB	VSS	Ground
C18	IRQ	DO	Interrupt output signal
C19	PWM1	AO	PWM1 output signal
C20	PWM0	AO	PWM0 output signal
C21	PWM2	AO	PWM2 output signal
C22	PWM_GND	VSS	Ground
C23	V3P3A_GNDA	VSS	Ground
C24	V3P3A_LX1A	AO	Buck boost V3P3A LX node 1
C25	V3P3A_INC	PS	V3P3A buck boost supply voltage
D1	VNN_IN1A	PS	VNN buck regulator supply voltage
D2	VNN_LX1A	AO	VNN buck LX node phase 1
D3	VNN_GND1B	PS	Ground

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
D4	VNN_GND2B	PS	Ground
D5	VNN_GND3B	PS	Ground
D6	VNN_GND4B	PS	Ground
D7	GPIO0_VDD	VSS	Ground
D8	V1P2A	AO	V1P2A output voltage
D9	V1P8SX	AO	V1P8SX output voltage
D10	V1P8U_FB	AI	V1P8U sense line
D11	V1P8U_EN_B	AO	V1P8U external FET control
D12	V1P8A_FBP	AI	Buck V1P8A sense line positive
D13	V1P8A_FBN	AI	Buck V1P8A sense line negative
D14	VDDQ_FBP	AI	Buck VDDQ sense line positive
D15	VDDQ_FBN	AI	Buck VDDQ sense line negative
D16	V2P85S_FBN	AI	Buck boost V2P85S sense line positive
D17	V2P85S_FBP	AI	Buck boost V2P85S sense line negative
D18	CHGDET_B	DI	USB charger detection input signal
D19	VHOST_EN	DO	VHOST enable signal
D20	VBUS_EN	DO	VBUS enable output signal
D21	PWM_VDD	AI	PWM input supply
D22	V3P3A_FBN	AI	Buck boost V3P3A sense line negative
D23	V3P3A_GNDB	VSS	Ground
D24	V3P3A_LX1B	AO	Buck boost V3P3A LX node 1
D25	V3P3A_INB	PS	V3P3A buck boost supply voltage
E1	DGND14	VSS	Ground
E2	DGND15	VSS	Ground
E3	GPIO0_GND	VSS	Ground
E4	VNN_FBP	AI	Buck VNN sense line positive
E5	GPIO0P4	ADIO	Low voltage GPIO 4
E6	GPIO0P3	ADIO	Low voltage GPIO 3
E7	GPIO0P2	ADIO	Low voltage GPIO 2
E8	GPIO0P1_BATIDOUT	ADIO	Low voltage GPIO 1

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
E9	GPIO0P0_BATIDIN	ADIO	Low voltage GPIO 0
E10	SUSPWRDNACK	DI	SUSPWRDNACK input signal
E11	SLP_S4_B	DI	SLP_S4_B input signal
E12	SLP_S0IX_B	DI	SLP_S0iX_B input signal
E13	SLP_S3_B	DI	SLP_S3_B input signal
E14	SDMMC3_PWR_EN_B	DI	SDMMC-card power enable
E15	SDMMC3_1P8_EN	DI	SDMMC-card power select
E16	PWRBTN_B	DO	Power button signal towards SoC
E17	PLTRST_B	DI	Platform reset signal
E18	DRAMPWROK	DO	DRAMPWROK output signal
E19	MODEM_OFF_B	DO	Modem off output signal
E20	CHGRINT_B		Interrupt input signal of external charger
E21	THERMTRIP_B		THERMTRIP_B output signal
E22	V3P3A_FBP	AI	Buck boost V3P3A sense line positive
E23	V3P3A_GNDC	VSS	Ground
E24	V3P3A_LX1C	AO	Buck boost V3P3A LX node 1
E25	V3P3A_INA	PS	V3P3A buck boost supply voltage
F1	SVID_DIO	DIO	SVID data signal
F2	I2C_DATA	DIO	I2C data signal
F3	DEBUG_SVID_DIO	DIO	Debug SVID data signal
F4	GPIO0P7	ADIO	Low voltage GPIO 7
F5	GPIO0P5	AD10	Low voltage GPIO 5
F6	DGND18	VSS	Ground
F7	DGND19	VSS	Ground
F8	DGND20	VSS	Ground
F9	DGND21	VSS	Ground
F10	DGND21	VSS	Ground
F11	DGND23	VSS	Ground
F12	DGND24	VSS	Ground
F13	DGND25	VSS	Ground

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
F14	DGND26	VSS	Ground
F15	DGND27	VSS	Ground
F16	DGND28	VSS	Ground
F17	DGND29	VSS	Ground
F18	DGND30	VSS	Ground
F19	DGND31	VSS	Ground
F20	DGND32	VSS	Ground
F21	DGND33	VSS	Ground
F22	V3P3S_FB	AI	V3P3S sense signal
F23	DGND8	VSS	Ground
F24	V3P3A_LX2A	AO	Buck boost V3P3A LX node 2
F25	V3P3A_C	AO	Buck boost V3P3A output voltage
G1	SVID_CLK	DI	SVID clock signal
G2	I2C_CLK	DI	I2C clock signal
G3	DEBUG_SVID_CLK	DI	Debug SVID clock signal
G4	DEBUG_SVID_ALERT_B	DO	Debug SVID alert signal
G5	GPIO0P6	ADIO	Low voltage GPIO 6
G6	DGND35	VSS	Ground
G7	DGND36	VSS	Ground
G8	DGND37	VSS	Ground
G9	DGND38	VSS	Ground
G10	DGND39	VSS	Ground
G11	DGND40	VSS	Ground
G12	DGND41	VSS	Ground
G13	DGND42	VSS	Ground
G14	DGND43	VSS	Ground
G15	DGND44	VSS	Ground
G16	DGND45	VSS	Ground
G17	DGND46	VSS	Ground
G18	DGND47	VSS	Ground

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
G19	DGND48	VSS	Ground
G20	DGND49	VSS	Ground
G21	VREFDQ1	AO	VREFDQ1 output voltage
G22	V3P3S_EN_B	AO	V3P3S external FET control signal
G23	DGND9	VSS	Ground
G24	V3P3A_LX2B	AO	Buck boost V3P3A LX node 2
G25	V3P3A_B	AO	Buck boost V3P3A output voltage
H1	SVID_ALERT_B	DO	SVID alert signal
H2	DEBUG_CS	DI	Debug interface selection signal
H3	DEBUG_I2C_CLK	DI	Debug I2C clock signal
H4	DEBUG_I2C_DATA	DIO	Debug I2C data signal
H5	GPIO1P6	ADIO	High voltage GPIO 6
H6	DGND51	VSS	Ground
H7	DGND52	VSS	Ground
H8	DGND53	VSS	Ground
H9	DGND54	VSS	Ground
H10	DGND55	VSS	Ground
H11	DGND56	VSS	Ground
H12	DGND57	VSS	Ground
H13	DGND58	VSS	Ground
H14	DGND59	VSS	Ground
H15	DGND60	VSS	Ground
H16	DGND61	VSS	Ground
H17	DGND62	VSS	Ground
H18	DGND63	VSS	Ground
H19	DGND64	VSS	Ground
H20	DGND65	VSS	Ground
H21	VREFDQ0	AO	VREFDQ0 output voltage
H22	V3P3U_FB	AI	
H23	DGND10	VSS	Ground

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
H24	V3P3A_LX2C	AO	Buck boost V3P3A LX node 2
H25	V3P3A_A	AO	Buck boost V3P3A output voltage
J1	DGND16	VSS	Ground
J2	DGND17	VSS	Ground
J3	VCC_GND1A	VSS	Ground
J4	GPIO1P7	ADIO	High voltage GPIO 7
J5	GPIO1P5	ADIO	High voltage GPIO 5
J6	GPIO1P4	ADIO	High voltage GPIO 4
J7	GPIO1P3	ADIO	High voltage GPIO 3
J8	GPIO1P2	ADIO	High voltage GPIO 2
J9	GPIO1P1	ADIO	High voltage GPIO 1
J10	GPIO1P0_UIBTN_B	ADIO	High voltage GPIO 0
J11	PROCHOT_B	DO	MYXPM6021 high temperature indication
J12	VREFT	AO	Reference thermistor output voltage
J13	VREFB	AO	Reference voltage battery ID measurement
J14	PWRBTNIN_B	AI	Power detection input signal
J15	VDCIN_SENSE	AI	DC input voltage detection
J16	ILIM1	DO	Charger current control signal 1
J17	ILIM0	DO	Charger current control signal 0
J18	ULPI_VBUS_EN	DI	Input signal controlling VBUS_EN signal
J19	RTC_POR		RTC power on reset indication
J20	RSMRST_B	DO	Resume reset output signal
J21	COREPWROK	DO	COREPWROK output signal
J22	V3P3U_EN_B	AO	V3P3U external FET control signal
J23	V1P8A	AO	V1P8A output supply
J24	BACKLIGHT_EN	DO	Backlight enable signal
J25	VSDIO_VIN	AI	VSDIO input power
K1	VCC_IN1A	PS	VCC buck regulator supply voltage
K2	VCC_LX1A	AO	VCC buck LX node phase 1
K3	VCC_GND1B	VSS	Ground

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
K4	VCC_FBN	AI	VCC buck sense line negative
K5	VCC_FBP	AI	VCC buck sense line positive
K6	GPIO1_GND	VSS	Ground
F7	GPIO1_VDD	ADIO	High voltage GPIO input supply
K8	V1P05S_FBN	AI	V1P05S buck sense line negative
K9	V1P05S_FBP	AI	V1P05S buck sense line positive
K10	VDDQ_VTT_R	AO	VDDQ_VTT reference output voltage
K11	VLP	AP	Low power regulator output voltage
K12	SYSTHERM0	AI	System thermistor 0 input
K13	VBUS_SENSE	AI	VBUS_SENSE input voltage detection
K14	SYSTHERM2	AI	System thermistor 2 input
K15	BPTHERM0	AI	Battery pack 0 thermistor input
K16	BPTHERM1	AI	Battery pack 1 thermistor input
K17	V5P0S_FBN	AI	V5P0S buck boost sense line negative
K18	V5P0S_FBP	AI	V5P0S buck boost sense line positive
K19	V1P0A_FBN	AI	V1P0A buck sense line negative
K20	V1P0A_FBP	AI	V1P0A buck sense line positive
K21	BATLOW_B	DO	Low battery detection output signal
K22	ACPRESENT	AI	Indication of availability of external supply
K23	PANEL_EN	DO	LCD panel enable signal
K24	VUSBPHY	AO	VUSBPHY output voltage
K25	VSDIO	AO	VSDIO output voltage
L1	VCC_IN1B	PS	VCC buck regulator supply voltage
L2	VCC_LX1B	AO	VCC buck LX node phase 1
L3	VCC_GND2A	VSS	Ground
L4	VCC_GND2B	VSS	Ground
L5	VCC_GND3A	VSS	Ground
L6	VCC_GND3B	VSS	Ground
L7	VCC_GND4A	VSS	Ground
L8	VCC_GND4B	VSS	Ground

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
L9	V1P05S_GND	VSS	Ground
L10	VDDQ_VTT_GND	VSS	Ground
L11	VLP_GND	VSS	Ground
L12	SYSTHERM1	AI	System thermistor 1 input
L13	V1P0SX_FB	AI	V1P0SX sense line
L14	VBAT_SENSE	AI	Battery voltage sense input signal
L15	VREF0P9	AO	0.9V reference output voltage
L16	VHDMI	AO	VHDMI output voltage
L17	V5P0S_GNDA	VSS	Ground
L18	V5P0S_GNDB	VSS	Ground
L19	V1P0A_GNDA	VSS	Ground
L20	V1P0A_GNDB	VSS	Ground
L21	BATID	DIO	Battery ID port
L22	VSYSU_FB	AI	VSYSU sense line
L23	VSYS_SX_FB	AI	VSYS_SX sense line
L24	VSYSU_EN_B	AO	VSYSU external FET control line
L25	VSYS_SX_EN_B	AO	VSYS_SX external FET control line
M1	VSYS11	PS	System power supply
M2	VSYS13	PS	System power supply
M3	VCC_LX2A	AO	VCC buck LX node phase 2
M4	VCC_LX2B	AO	VCC buck LX node phase 2
M5	VCC_LX3A	AO	VCC buck LX node phase 3
M6	VCC_LX3B	AO	VCC buck LX node phase 3
M7	VCC_LX4A	AO	VCC buck LX node phase 4
M8	VCC_LX4B	AO	VCC buck LX node phase 4
M9	V1P05S_LX	AO	Buck V1P05S LX node
M10	VSYS_3	PS	System power supply
M11	VDDQ_VTT	AO	VDDQ_VTT output voltage
M12	VSYS_2	PS	System power supply
M13	V1P0S_FB	AI	V1P0S sense line

Table 59: MYXPM6021 Ball Order (continued)

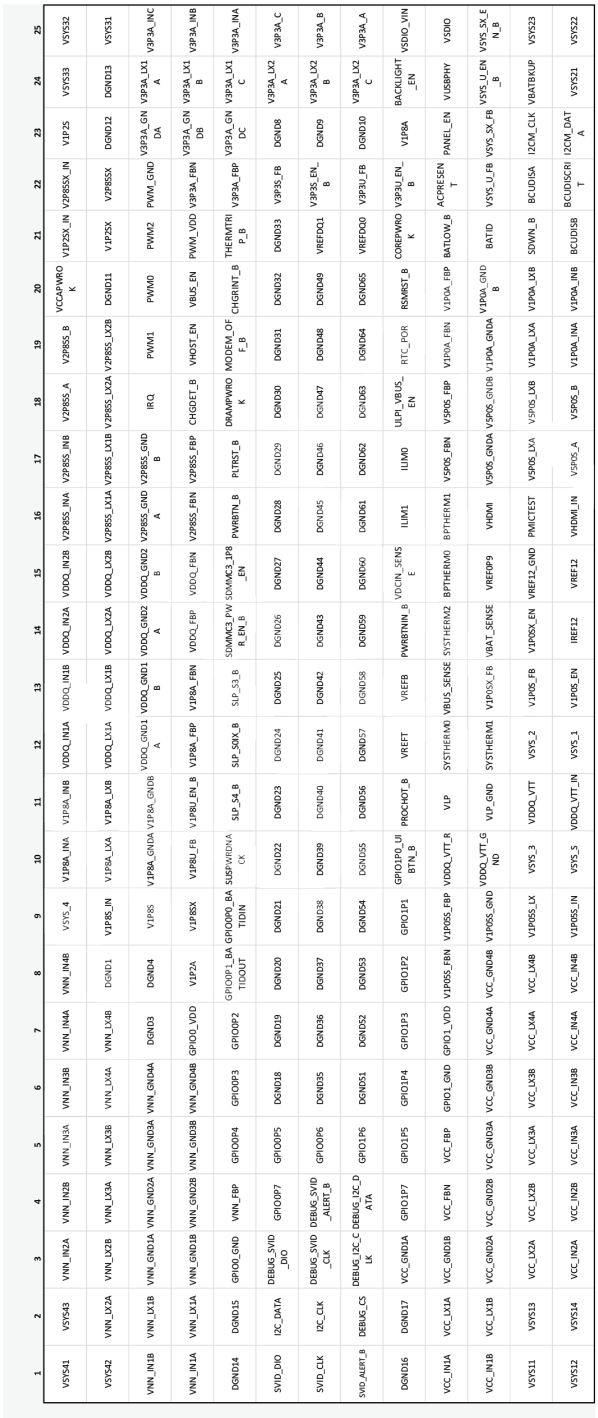
Ball	Name	Type	Description
M14	V1P0SX_EN	AO	V1P0SX external FET control line
M15	VREF12_GND	VSS	Ground
M16	PMICTEST	DI	Test signal
M17	V5P0S_LXA	AO	V5P0S buck boost LX node 1
M18	V5P0S_LXB	AO	V5P0S buck boost LX node 1
M19	V1P0A_LXA	AO	V5P0S buck boost LX node 2
M20	V1P0A_LXB	AO	V5P0S buck boost LX node 2
M21	SDWN_B	DO	Shut down warning output signal
M22	BCUDISA	DO	System voltage in warning zone A
M23	I2CM_SCL	DO	EEPROM clock signal
M24	VBATBKUP		Coin cell battery supply
M25	VSYS23	PS	System power supply
N1	VSYS12	PS	System power supply
N2	VSYS14	PS	System power supply
N3	VCC_IN2A	PS	VCC buck regulator supply voltage
N4	VCC_IN2B	PS	VCC buck regulator supply voltage
N5	VCC_IN3A	PS	VCC buck regulator supply voltage
N6	VCC_IN3B	PS	VCC buck regulator supply voltage
N7	VCC_IN4A	PS	VCC buck regulator supply voltage
N8	VCC_IN4B	PS	VCC buck regulator supply voltage
N9	V1P05S_IN	PS	Buck V1P05S input supply
N10	VSYS_S	PS	System power supply
N11	VDDQ_VTT_IN	AI	VDDQ_VTT input supply
N12	VSYS_1	PS	System power supply
N13	V1P0S_EN	AO	V1P0S external FET control signal
N14	IREF12		Bandgap current reference output
N15	VREF12	AO	Bandgap voltage reference output
N16	VHDMI_IN	AI	VHDMI supply voltage
N17	V5P0S_A	AO	V5P0S buck boost output voltage

Table 59: MYXPM6021 Ball Order (continued)

Ball	Name	Type	Description
N18	V5P0S_B	AO	V5P0S buck boost output voltage
N19	V1P0A_INA	PS	Buck V1P0A input supply
N20	V1P0A_INB	PS	Buck V1P0A input supply
N21	BCUDISB	DO	System voltage in warning zone B
N22	BCUDISCRIT	DO	System voltage in critical range
N23	I2CM_SDA	DI	EEPROM data signal
N24	VSYS21	PS	System power supply
N25	VSYS22	PS	System power supply

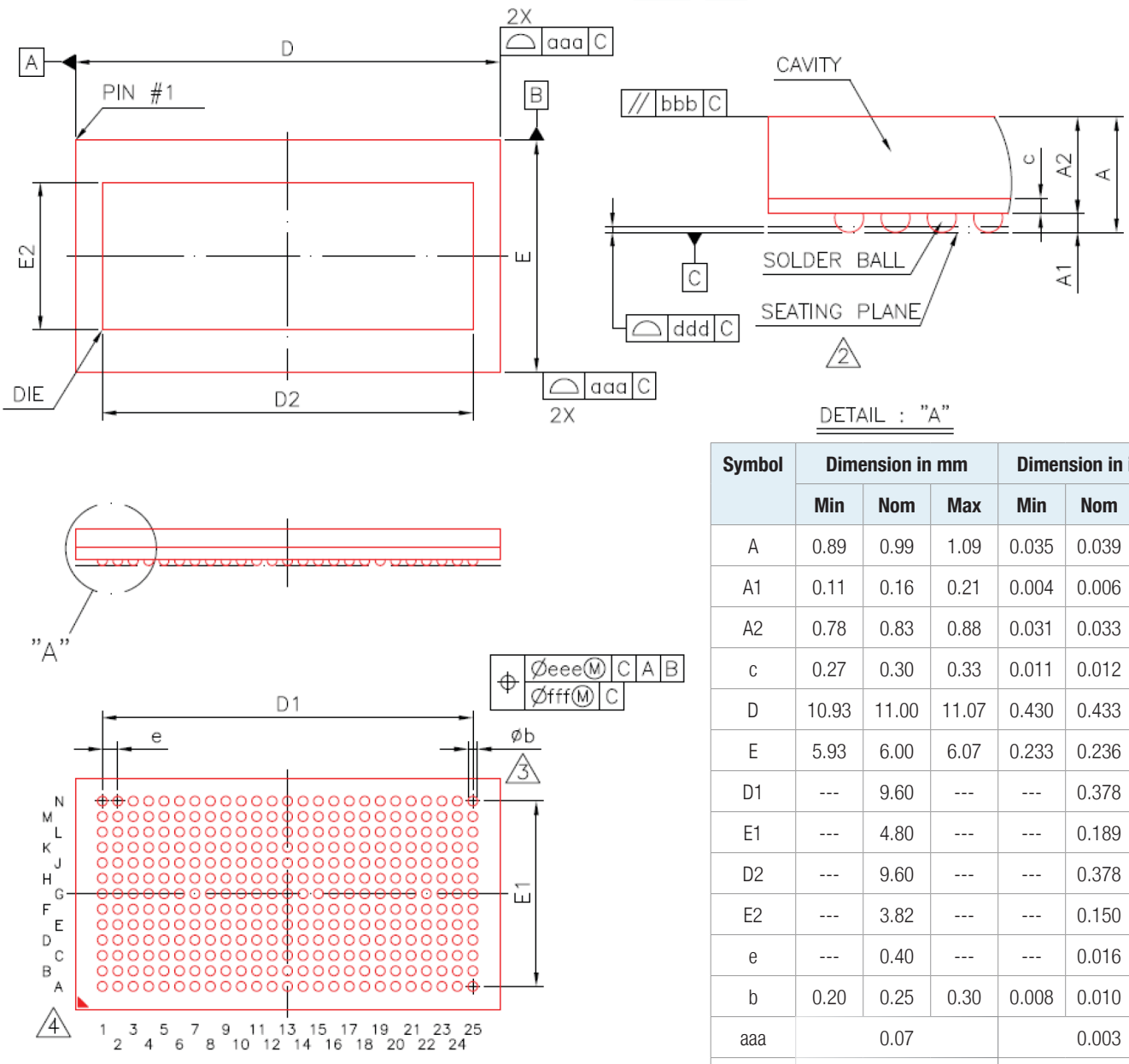
22.2 MYXPM6021 325 Pin FCBGA Package

Map of ball allocations as seen from above the package.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	V5YS41	V5YS43	VNN_IN2A	VNN_IN2B	VNN_IN3A	VNN_IN3B	VNN_IN4A	VNN_IN4B	V5YS_4	V1P8A_INA	V1P8A_INB	VDDQ_IN1A	VDDQ_IN1B	VDDQ_IN2A	VDDQ_IN2B	V2P85S_INA	V2P85S_INB	V2P85S_A	V2P85S_B	VCCAPWROK	V1P2SX_IN	V2P85SX_IN	V1P2S	V5YS33	V5YS32
B	V5YS42	VNN_LX2A	VNN_LX2B	VNN_LX3A	VNN_LX3B	VNN_LX4A	VNN_LX4B	DGND1	V1P8S_IN	V1P8A_LXA	V1P8A_LXB	VDDQ_LX1A	VDDQ_LX1B	VDDQ_LX2A	VDDQ_LX2B	V2P85S_LX1A	V2P85S_LX1B	V2P85S_LX2A	V2P85S_LX2B	DGND11	V1P2SX	V2P85SX	DGND12	DGND13	V5YS31
C	VNN_IN1B	VNN_LX1B	VNN_GND1A	VNN_GND2A	VNN_GND3A	VNN_GND4A	DGND3	DGND4	V1P8S	V1P8A_GNDA	V1P8A_GNDB	VDDQ_GND1A	VDDQ_GND1B	VDDQ_GND2A	VDDQ_GND2B	V2P85S_GNDA	V2P85S_GNDB	IRQ	PWM1	PWM0	PWM2	PWM_GND	V3P3A_GNDA	V3P3A_LX1A	V3P3A_INC
D	VNN_IN1A	VNN_LX1A	VNN_GND1B	VNN_GND2B	VNN_GND3B	VNN_GND4B	GPIO0_VDD	V1P2A	V1P8SX	V1P8U_FB	V1P8U_EN_B	VDDQ_FBP	V1P8A_FBN	VDDQ_FBP	VDDQ_FBN	V2P85S_FBP	V2P85S_FBN	CHGDET_B	VHOST_EN	VBUS_EN	PWM_VDD	V3P3A_FBN	V3P3A_GNDB	V3P3A_LX1B	V3P3A_INB
E	DGND14	DGND15	GPIO0_GND	VNN_FBP	GPIO0P4	GPIO0P3	GPIO0P2	GPIO0P1_BA TIDOUT	GPIO0P0_BA TIDIN	SUSPWRDNACK	SLP_S4_B	VDDQ_GND1A	SLP_S3_B	SDMMC3_PWR_EN_B	SDMMC3_IP8_EN	PWRBTN_B	PLTRST_B	DNAMPWROK	MODEM_OFF_B	CHGRINT_B	THERMTRIP_B	V3P3A_FBP	V3P3A_GNDC	V3P3A_LX1C	V3P3A_INA
F	SVID_DIO	I2C_DATA	DEBUG_SVID_DIO	GPIO0P7	GPIO0P5	DGND18	DGND19	DGND20	DGND21	DGND22	DGND23	DGND24	DGND25	DGND26	DGND27	DGND28	DGND29	DGND30	DGND31	DGND32	DGND33	V3P3S_FB	DGND8	V3P3A_LX2A	V3P3A_C
G	SVID_CLK	I2C_CLK	DEBUG_SVID_CLK	DEBUG_SVID_ALERT_B	GPIO0P6	DGND35	DGND36	DGND37	DGND38	DGND39	DGND40	DGND41	DGND42	DGND43	DGND44	DGND45	DGND46	DGND47	DGND48	DGND49	VREFDQ1	V3P3S_FBN_B	DGND9	V3P3A_LX2B	V3P3A_B
H	SVID_ALERT_B	DEBUG_CS	DEBUG_I2C_CLK	DEBUG_I2C_DATA	GPIO1P6	DGND51	DGND52	DGND53	DGND54	DGND55	DGND56	DGND57	DGND58	DGND59	DGND60	DGND61	DGND62	DGND63	DGND64	DGND65	VREFDQ0	V3P3U_FB	DGND10	V3P3A_LX2C	V3P3A_A
J	DGND16	DGND17	VCC_GND1A	GPIO1P7	GPIO1P5	GPIO1P4	GPIO1P3	GPIO1P2	GPIO1P1	GPIO1P0_UIBTN_B	PROCHOT_B	VREFT	VREFB	PWRBTNIN_B	VDCIN_SENSE	ILIM1	IUM0	ULPI_VBUS_EN	RTC_POR	RSMRST_B	V3P3U_FBN_B	V1P8A	BACKLIGHT_EN	VSDIO_VIN
K	VCC_IN1A	VCC_LX1A	VCC_GND1B	VCC_FBN	VCC_GND3A	VCC_GND3B	GPIO1_GND	GPIO1_VDD	V1P0S_FBP	VDDQ_VTT_R	VLP	SYSTHERM0	VBUS_SENSE	SYSTHERM2	BPTHERM0	BPTHERM1	V5P0S_FBN	V1P0A_FBN	V1P0A_FBP	BATLOW_B	ACPRESENT	PANEL_EN	VLSBPHY	VSDIO
L	VCC_IN1B	VCC_LX1B	VCC_GND2A	VCC_GND2B	VCC_GND3A	VCC_GND3B	VCC_LX4A	VCC_LX4B	V1P0S_GND	VDDQ_VTT_GND	VLP_GND	SYSTHERM1	V1P0S_FB	VBAT_SENSE	VREF0P9	VHDMI	V5P0S_GNDA	V5P0S_GNDB	V1P0A_GNDA	V1P0A_GNDB	BATID	V5YS_U_FB	V5YS_SX_FB	V5YS_U_EN_B	V5YS_SX_EN_B
M	V5YS11	V5YS13	VCC_LX2A	VCC_LX2B	VCC_LX3A	VCC_LX3B	VCC_LX4A	VCC_LX4B	V1P0S_LX	V5YS_3	VDDQ_VTT	V5YS_2	V1P0S_FB	V1P0SX_EN	VREF12_GND	PMICTEST	V5P0S_LXA	V5P0S_LXB	V1P0A_LXA	V1P0A_LXB	SDWN_B	BCUDISA	I2CM_CLK	VBATBKUP	V5YS23
N	V5YS12	V5YS14	VCC_IN2A	VCC_IN2B	VCC_IN3A	VCC_IN3B	VCC_IN4A	VCC_IN4B	V1P0S_IN	V5YS_5	VDDQ_VTT_IN	V5YS_1	V1P0S_EN	IREF12	VREF12	VHDMI_IN	V5P0S_A	V5P0S_B	V1P0A_INA	V1P0A_INB	BCUDISB	BCUDISCRIT	I2CM_DATA	V5YS21	V5YS22

22.3 Package Outline (325 pin, FCBGA 11x6mm, 0.4mm pitch)



Symbol	Dimension in mm			Dimension in inches		
	Min	Nom	Max	Min	Nom	Max
A	0.89	0.99	1.09	0.035	0.039	0.043
A1	0.11	0.16	0.21	0.004	0.006	0.008
A2	0.78	0.83	0.88	0.031	0.033	0.035
c	0.27	0.30	0.33	0.011	0.012	0.013
D	10.93	11.00	11.07	0.430	0.433	0.436
E	5.93	6.00	6.07	0.233	0.236	0.239
D1	---	9.60	---	---	0.378	---
E1	---	4.80	---	---	0.189	---
D2	---	9.60	---	---	0.378	---
E2	---	3.82	---	---	0.150	---
e	---	0.40	---	---	0.016	---
b	0.20	0.25	0.30	0.008	0.010	0.012
aaa		0.07			0.003	
bbb		0.10			0.004	
ddd		0.08			0.003	
eee		0.10			0.004	
fff		0.05			0.002	
MD/ME		25/13			25/13	

*Advanced information. Subject to change without notice.

Revision History

Revision #	History	Release Date	Status
1.0	Initial Release	September 2014	Preliminary
1.1	Added ECN #	October 20, 2014	Preliminary